Flash Memory Summit

Characterization of 3D NAND Flash Memories beyond 1GT/s

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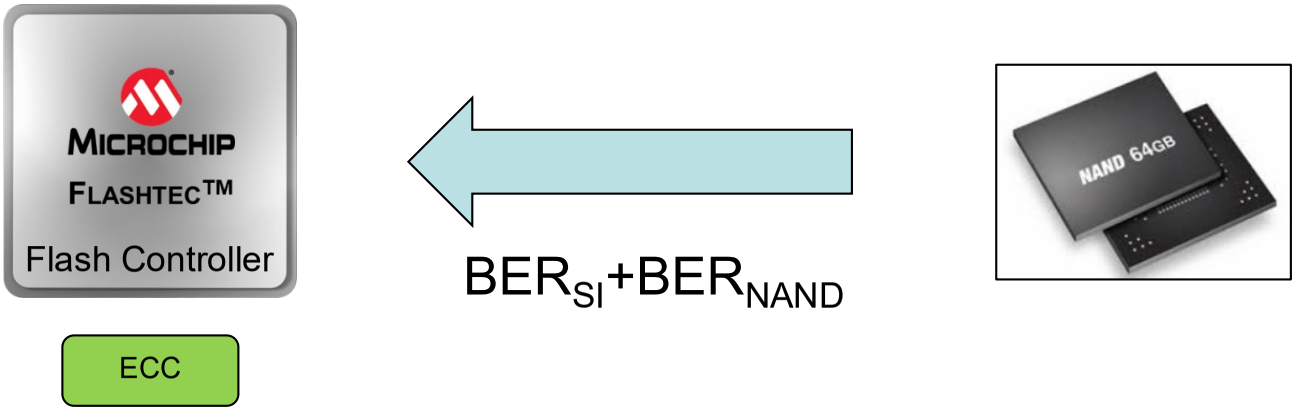
Background

- The request for more and more performant SSDs is pushing Flash manufacturers to increase the I/O speed of NAND memories.
- Indeed, we start seeing in the market both ONFI and Toggle NAND devices capable of running their interface beyond 1GT/s.
- Needless to say that, in the near future, the transition to PCIe Gen5 will probably translate into a need for even higher speeds.
- From a design perspective, the most obvious consequence of high speed is Signal Integrity, which implies a more careful design of the entire PCB inside the SSD case.

Problem Statement

- But this presentation addresses another aspect: NAND reliability at high speed.
- As the transfer rate goes up, I/O circuits consume more power and inject more noise in the surrounding circuits: what's the impact on NAND raw BER, especially at the End of Life, i.e. when distributions get closer to each other?

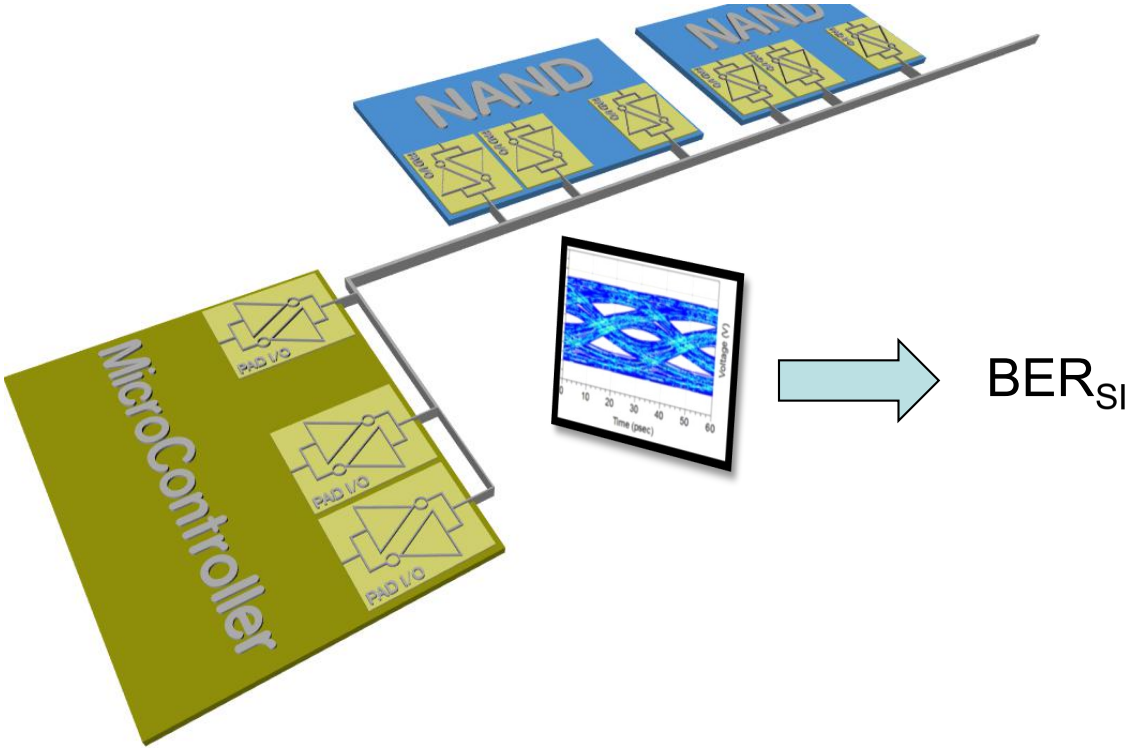
BER



- ECC can't distinguish between BER_{NAND} and BER_{SI} (ECC sits on the controller side) -> Signal Integrity needs to be optimized

Signal Integrity

- High speed design implies Signal Integrity optimization to reduce BER_{SI}



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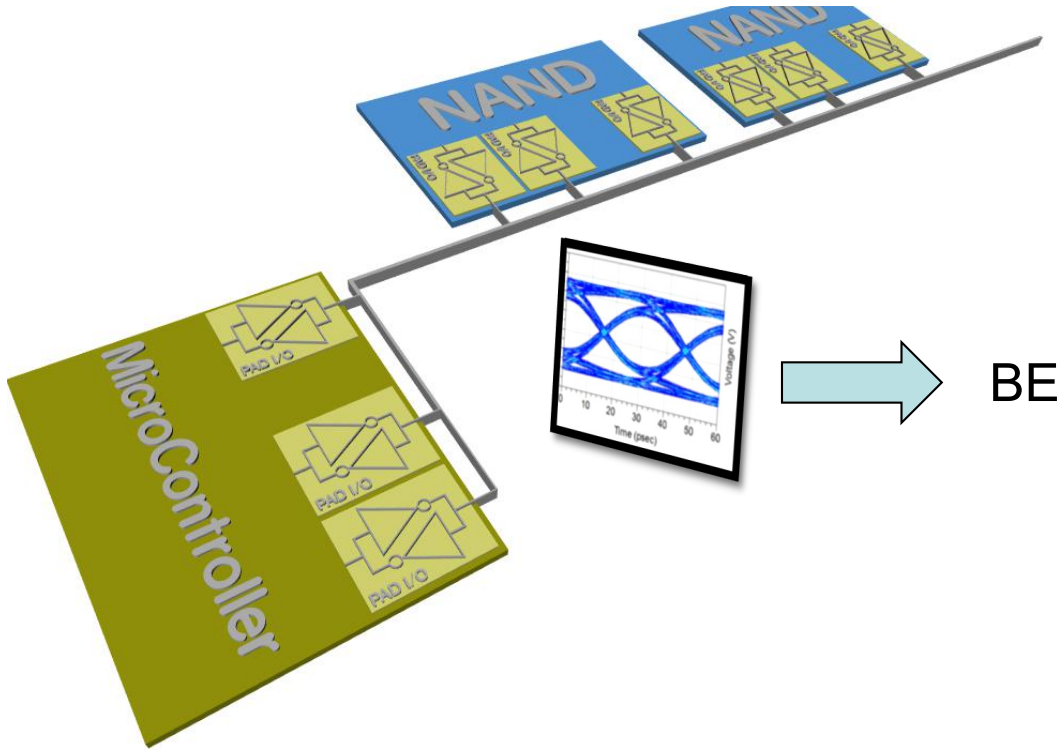

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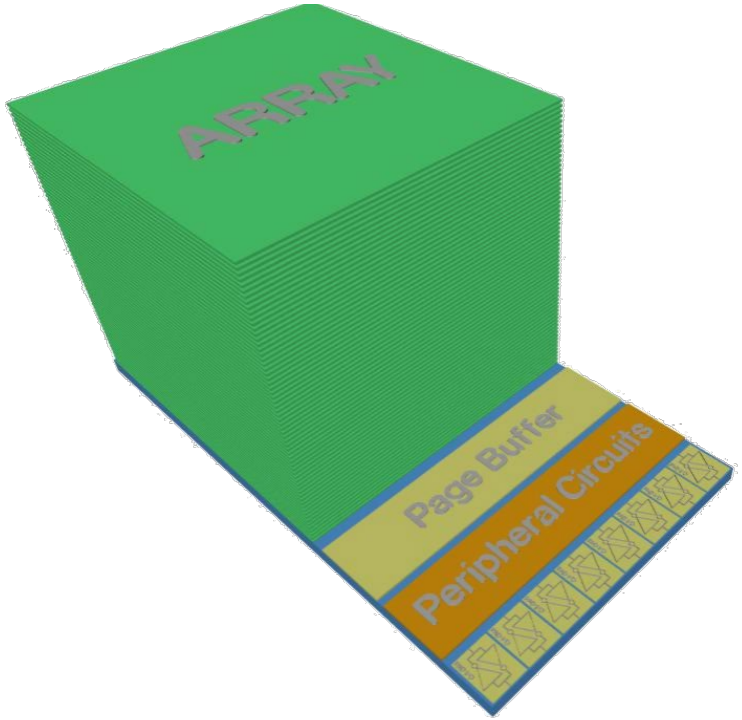
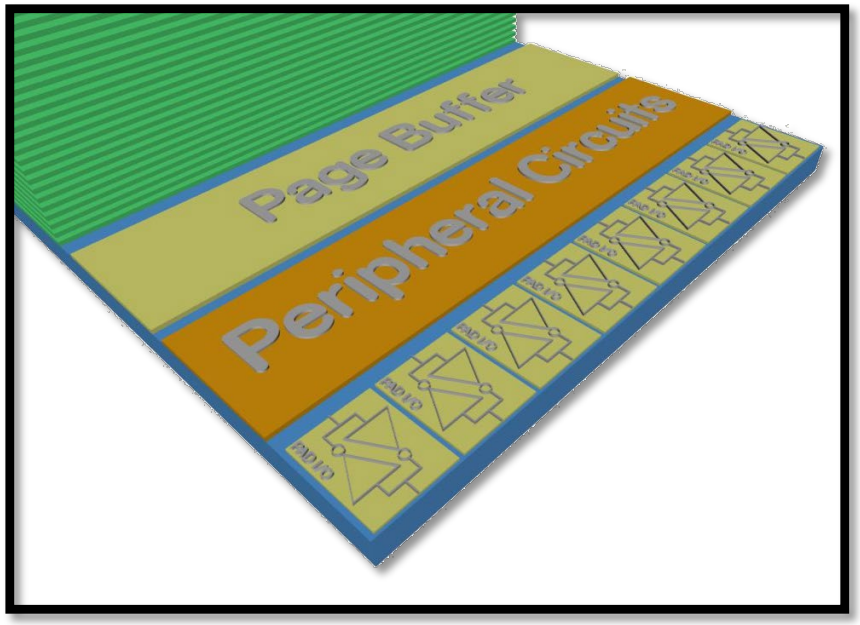
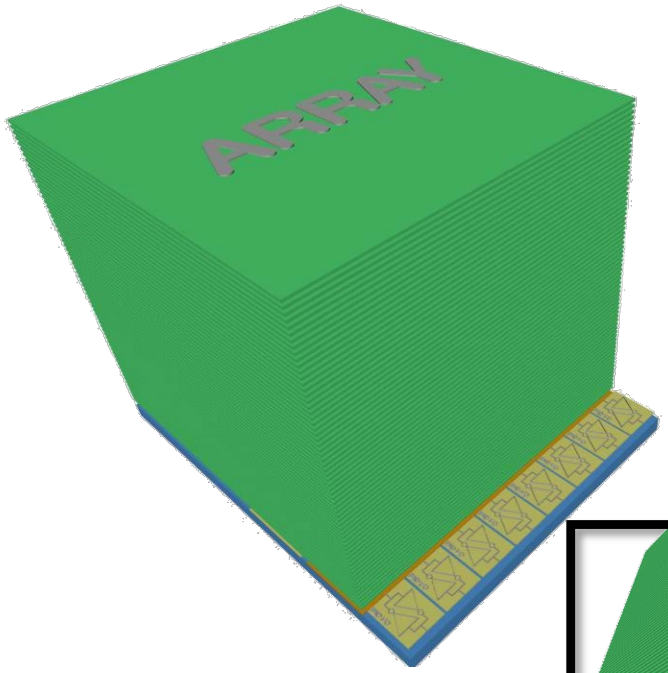
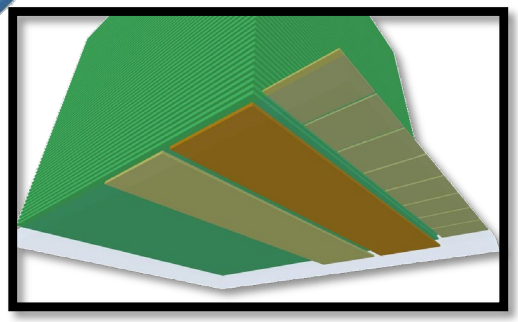
3D NAND

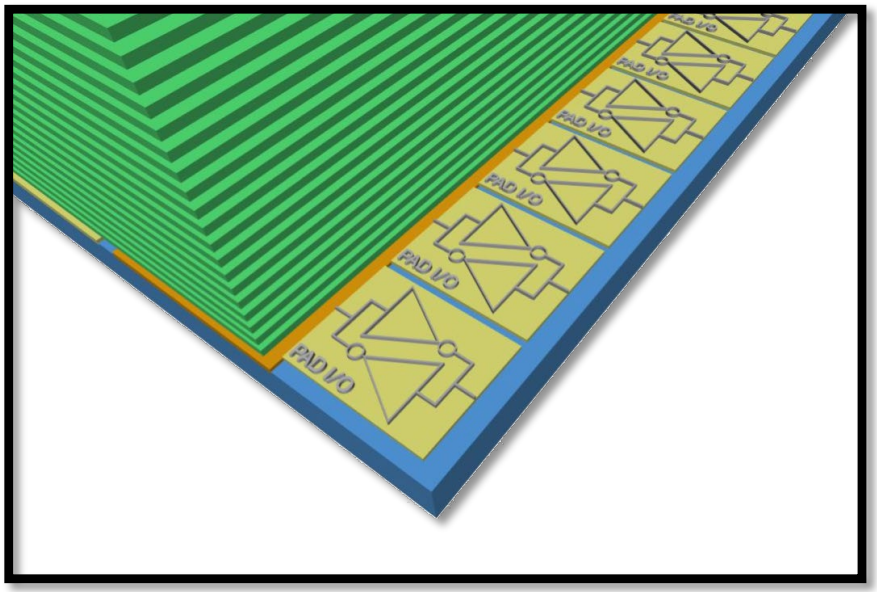




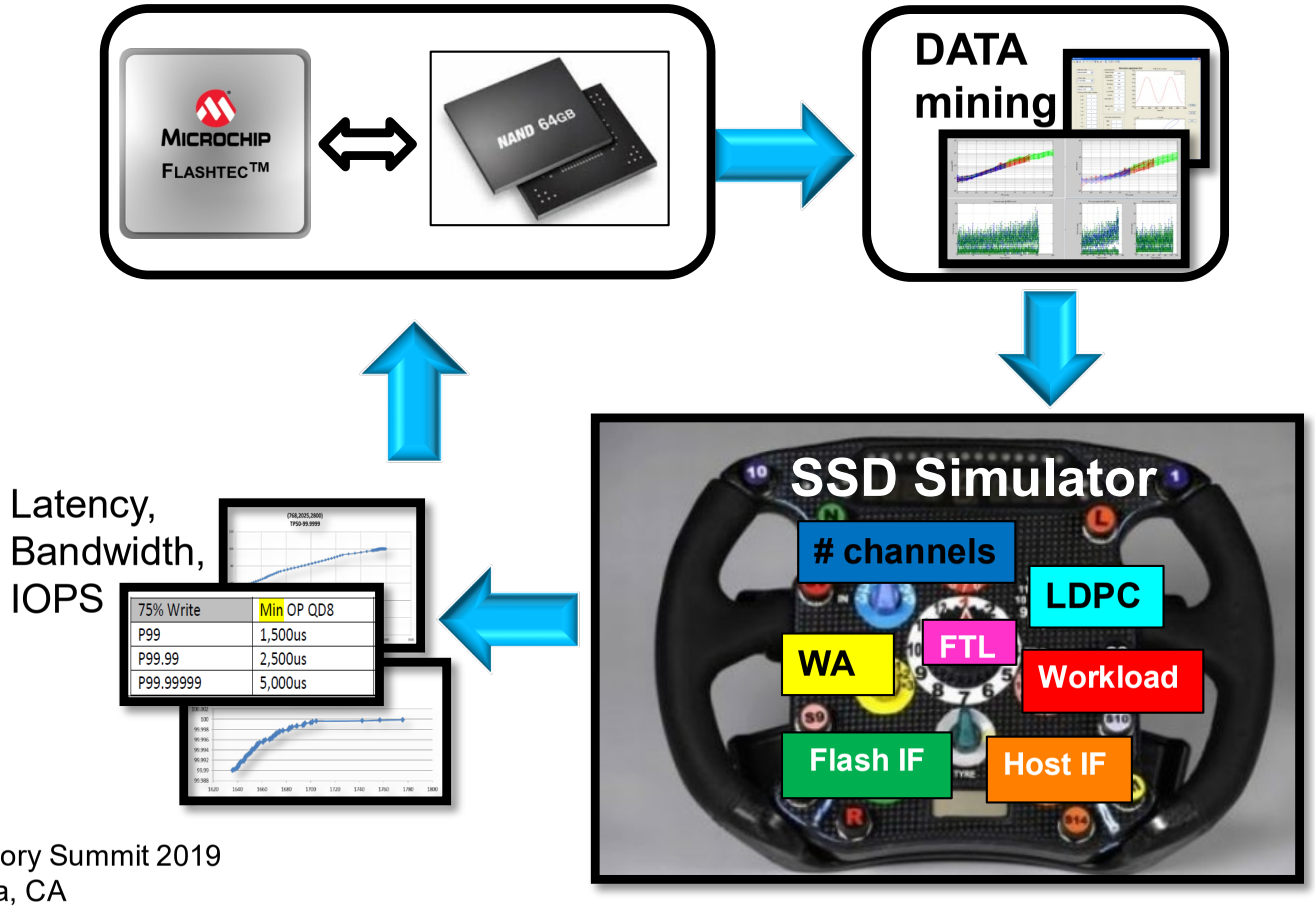
3D NAND – Circuits Under Array







Fully Integrated SSD-NAND Characterization Flow



Testing at High I/O Speed

- Is BER_{NAND} a function of the I/O speed?
- To answer this question we performed the entire NAND reliability analysis by running the NAND at the maximum speed.

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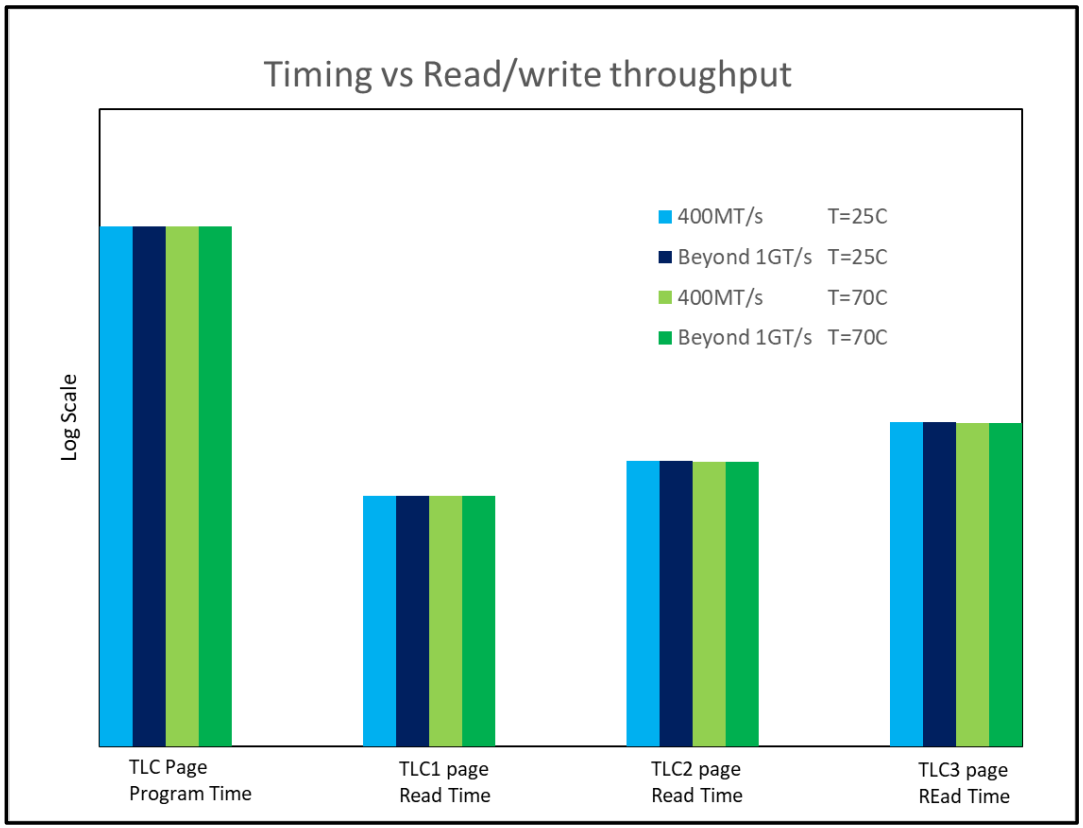
Timing



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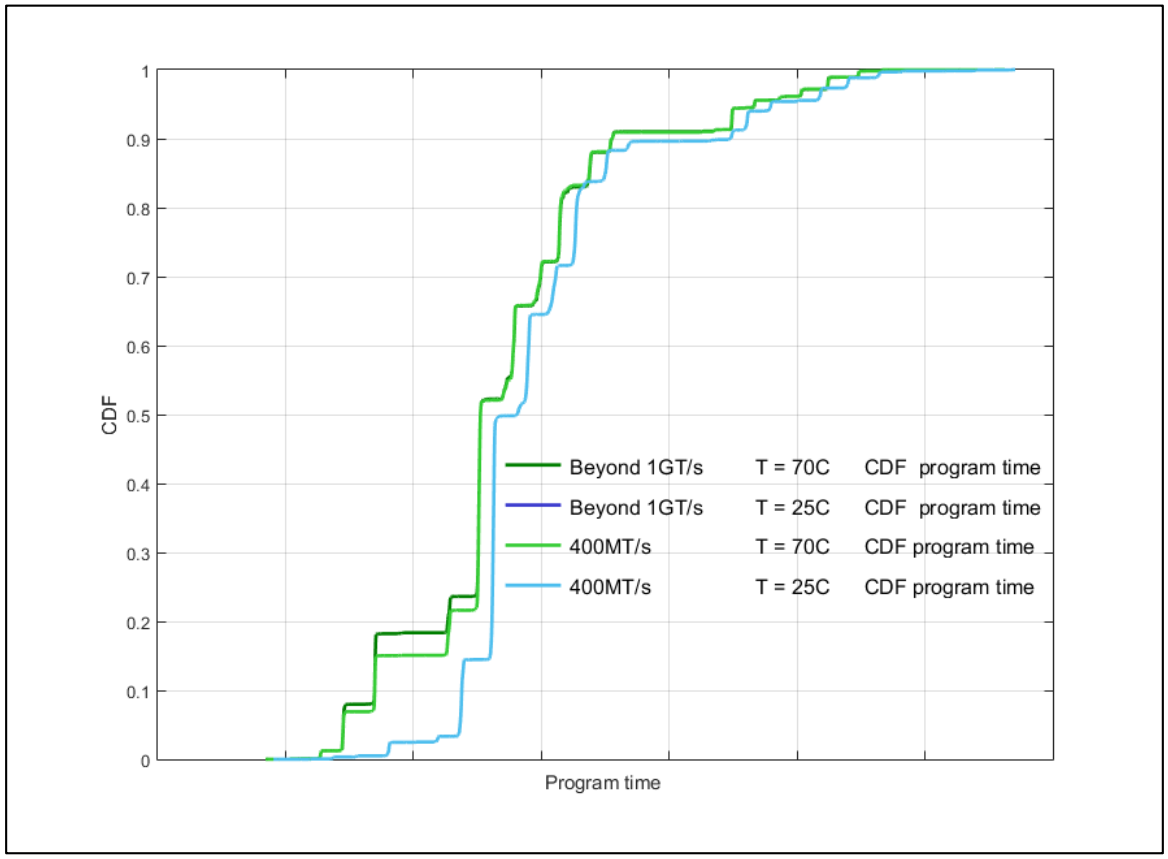
CDF Program time



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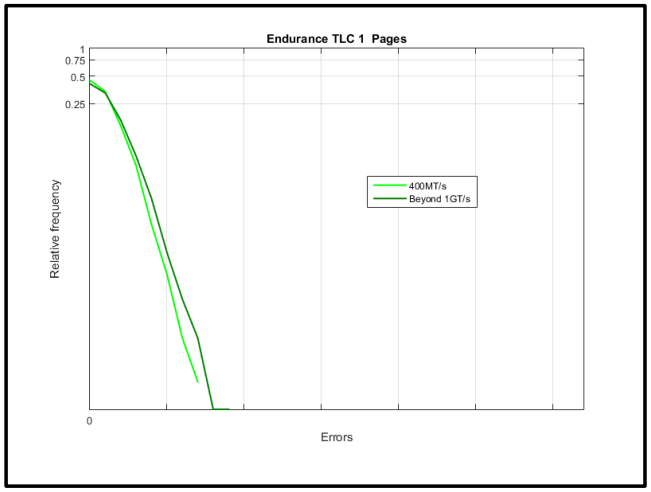
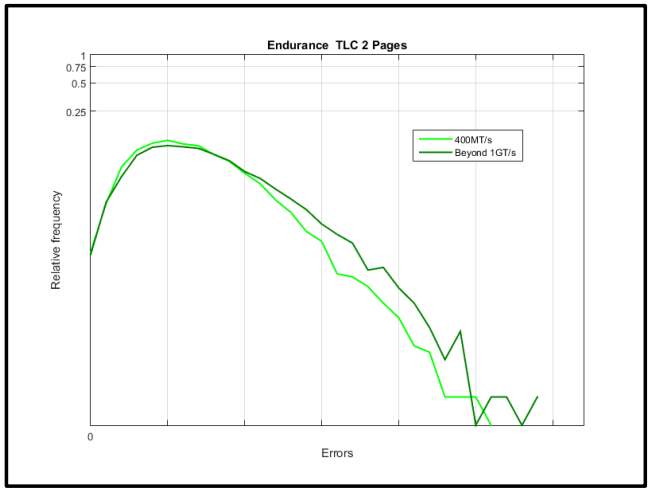
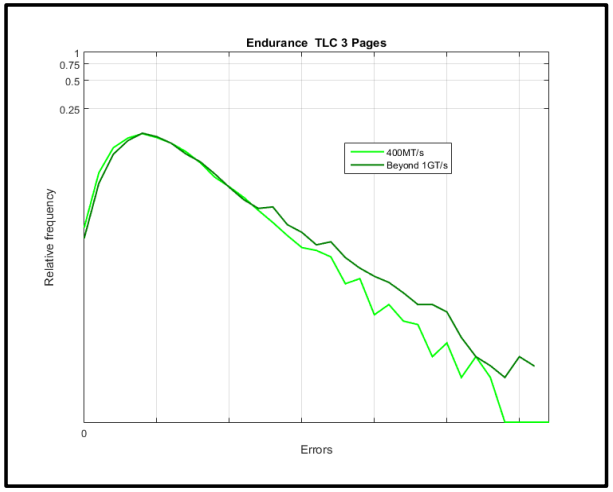
Errors after Endurance







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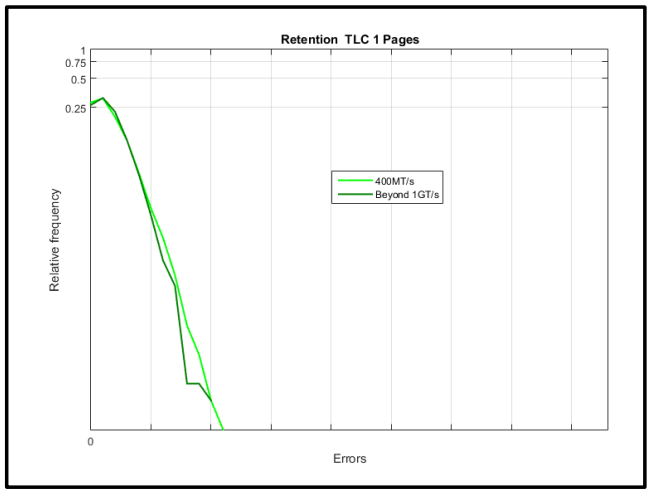
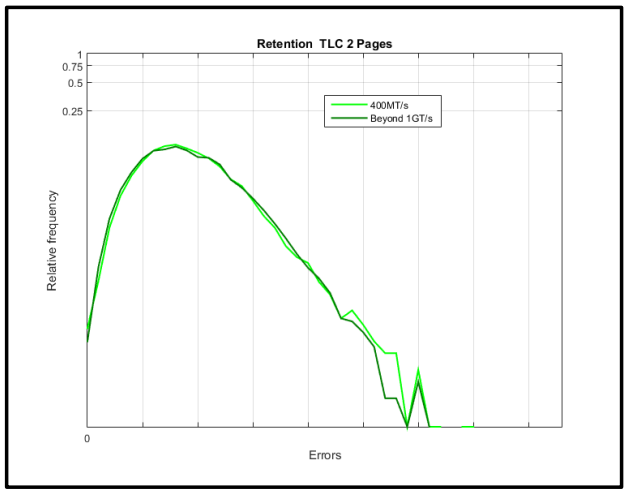
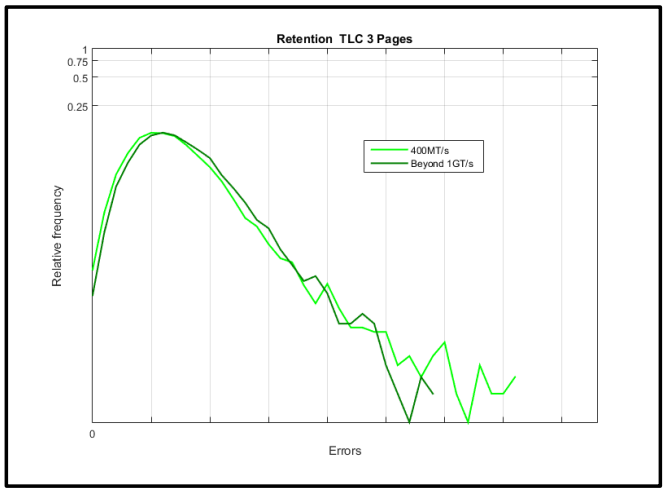
Errors after Retention







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Conclusions

- NAND I/O speed has crossed the 1GT/s boundary, and it is expected to grow even more (PCIe Gen5)
- High-performance SSD controllers need to support 1GT/s+
- Both SSD Controller and NAND need to optimize how they capture and send signals -> SSD Controller flexibility is key.
- Signal Integrity at the board level has to be carefully designed
- NAND characterization has to be done at speed to verify that there is no impact on BER at EOL
- The first set of experiments show that Endurance is not impacted by I/O speed if Signal Integrity is optimized

Thank You

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