

pSLC Cache Design for Enhanced Performance and Lifetime

Thomas W. McCormick Chief Engineer/Technologist



Santa Clara, CA August 2019



- "Fixed function system"
 - Telecom, automotive, industrial control systems, medical equipment ...
- Commonality: Flash Storage
 - Code & data









[Wikipedia – Creative Commons]



- Smaller process, more bits per cells
 - Endurance & ECC
 - Retention
- Challenge: Maintain acceptable service-life for embedded systems



Lifetime (P/E Cycles)





[Mark Richards, Computer History Museum]







- Still a flat memory space (mostly)
- Each layer is a cache
- Cache design is critical
 - Performance issues for misses







	pSLC	TLC
Speed	+3x	1x
Cost	-3x	1x
Endurance	20K (~7x)	3K



- pSLC Cache (Fastest) All pSLC
- pSLC Enabled (?) Blended
- TLC Enabled (Slowest ?) All TLC











- pSLC Cache (Fastest) 100%
- pSLC Enabled (Slowest!) 30%
 - Widely varying performance (>10x)
- TLC Enabled 35%





Drive Lifetime



- pSLC Cache
 - Improved burst performance (up to 100% pSLC)
 - Reduced sustained performance (lower than TLC)
 - Workload dependant











pSLC is 1/3 storage (512 GB -> 170 GB) What about 1/4 storage (512 GB -> 128 GB)?













pSLC Cache

- Improved burst performance (up to 100% pSLC)
- Reduced sustained performance (lower than TLC)
- pSLC (100%)
 - Improved burst and sustained performance
 - 8x drive lifetime
 - True SLC drive size



- Flash Memory System Embedded Events:
 - Embedded Applications, Part 1 (101-B)
 - Tues 8:30 9:35 AM
 - Embedded Applications, Part 2 (102-B)
 - Tues 9:45 10:50 AM
 - Beer, Pizza, and Chat with the Experts
 - Tues 7:00 8:30 PM
 - Flash and the IoT (302-B)
 - Thurs 3:40 5:00 PM



Tom McCormick - Chief Engineer/Technologist Swissbit tom.mccormick@swissbit.com











