



Flash Memory Summit



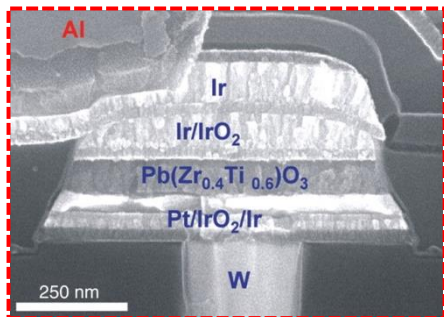
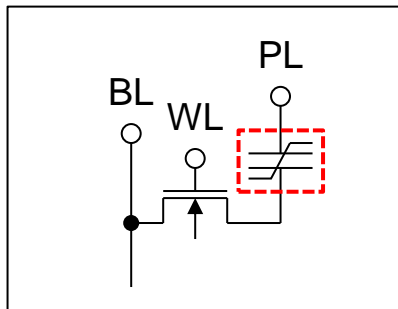
# FeFET Memory: (e)NVM for Advanced Technology Nodes

Dr. Stefan Müller (Ferroelectric Memory Co.)



# FeFET is not FRAM!

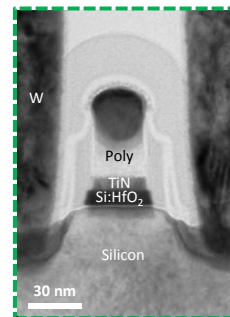
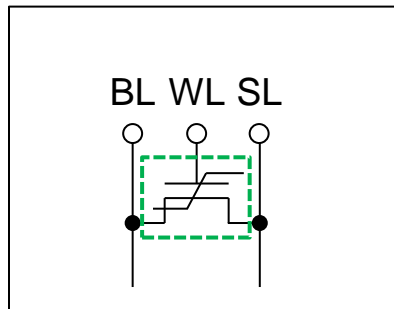
What I **not** going to talk about:  
Classical 1T-1C **FRAM**



Source: Science, Vol. 315, pp. 954-959

- 1T-1C memory cell
- Exotic ferroelectric materials (PZT)
- Stuck at 130 nm

What I **am** going to talk about:  
Novel 1T **FeFET**



Source: S. Mueller, EMF, 2015.

- + 1T memory cell
- + **Ferroelectric HfO<sub>2</sub>**
- + In dev. at 22 nm

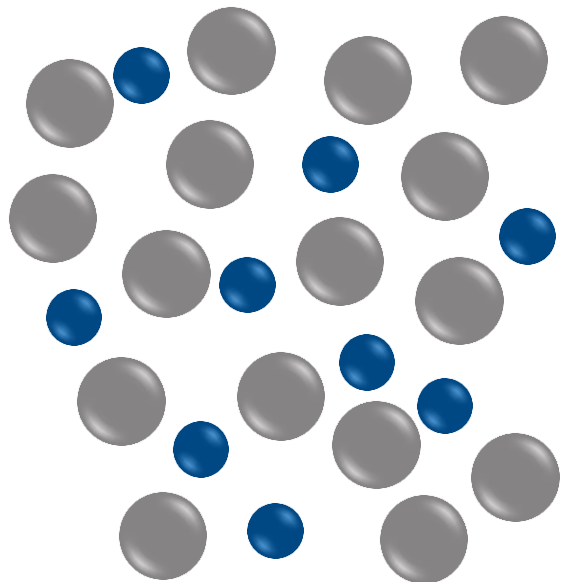
to actual scale...



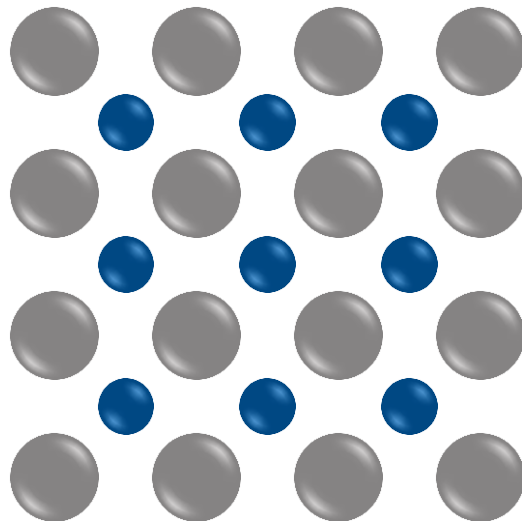
**THE enabler for FeFET!**



# Ferroelectric $\text{HfO}_2$



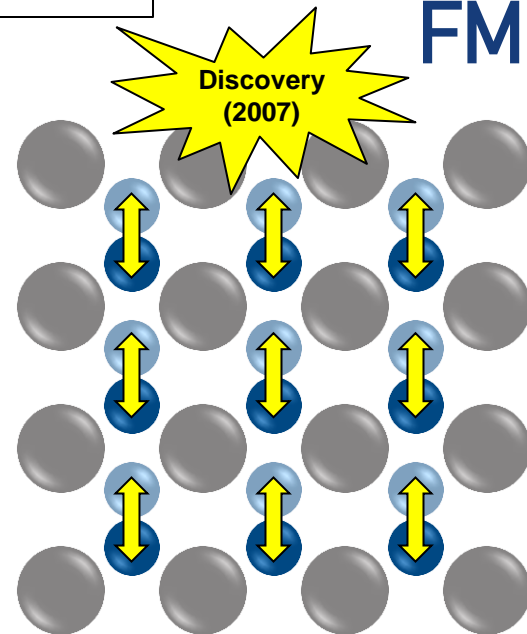
Amorphous (unordered)  $\text{HfO}_2$   
(used in **CMOS** gate stack)



Crystalline (ordered)  $\text{HfO}_2$   
(used in **DRAM** capacitor)

\*Actually  $\text{ZrO}_2$  but chemically almost identical

Dr. Stefan Müller (CEO)

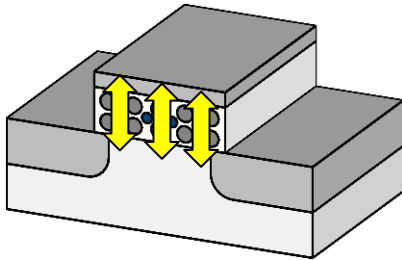


**Ferroelectric  $\text{HfO}_2$**   
**2 atom positions = 1 Bit!**  
**(Patented)**

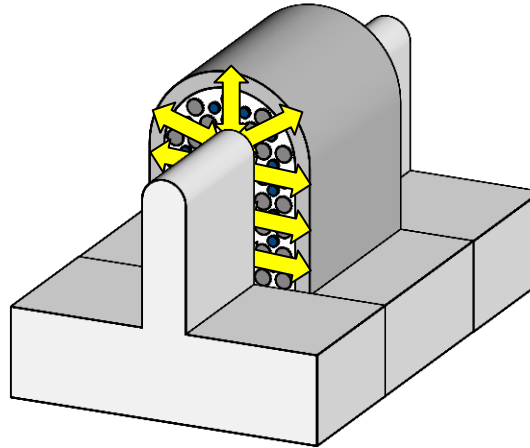


# Why it matters

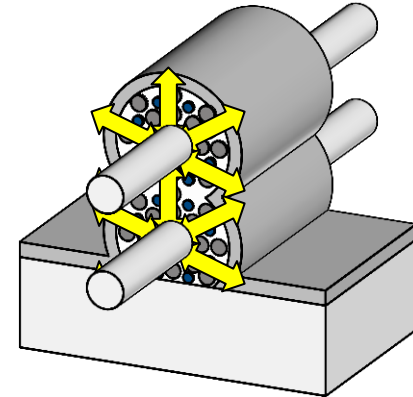
Planar transistor  
( $> 20$  nm)



Fin-transistor  
( $20$  nm –  $7$  nm, today)



Nanowire-transistor  
( $< 7$  nm, future)

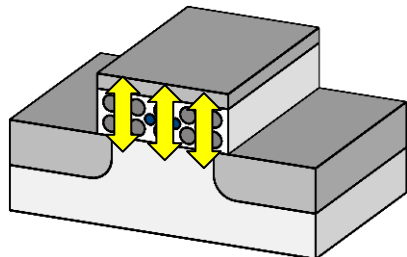





We transform any logic transistor into a memory cell! (2 threshold voltage states)



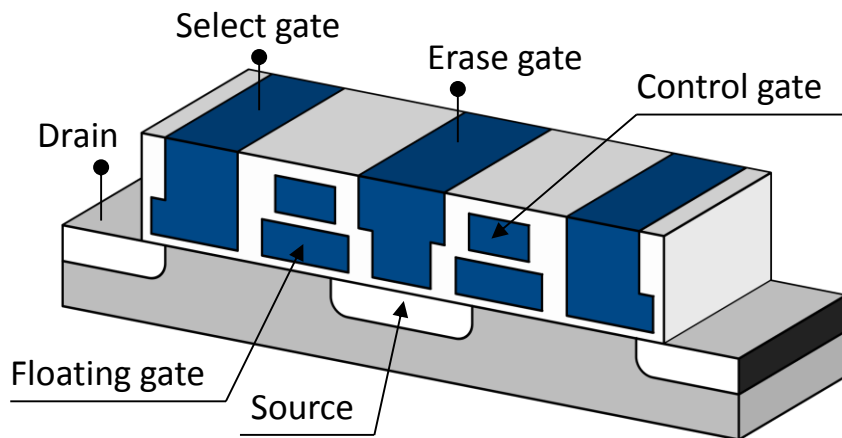
# FeFET vs. eFlash




## FeFET:



-  2 additional masks
-  Write voltage 2V ... 4V
-  Write by gate voltage only

## eFlash (2 bit):

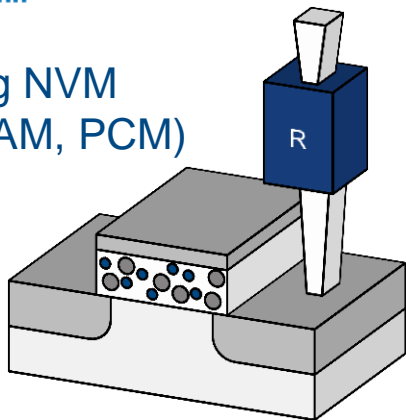


-  15+ additional masks
-  Write voltage > 10V
-  Write by channel current flow (HCI)

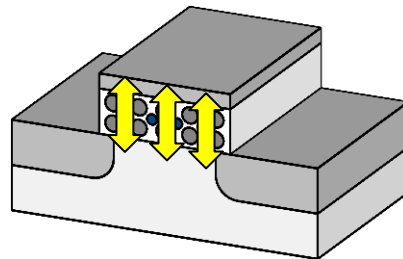


# FeFET vs. emerging NVM

Emerging NVM  
(RRAM, MRAM, PCM)



The FeFET solution



## Challenges:

- **Additional memory element R adds cost!**
- Higher power consumption
- Questionable scalability

## FeFET benefits:

- Reduces manufacturing cost significantly
- Lowers power consumption by 1000x
- Inherently scalable alongside CMOS



# Technology status

	FeFET array (IEDM '16 & '17)	Lab capacitor	Theory
Cell size	44F <sup>2</sup> (0.035 μm <sup>2</sup> ) planar AND-type	> 10.000 μm <sup>2</sup>	< 4F <sup>2</sup> (3D)
Write speed	10 ns	10 ns	< 1 ns
Read speed	20 ns (limited by design)	10 ns	< 1 ns (architecture)
Endurance	10 <sup>5</sup> cycles	> 10 <sup>10</sup> cycles	Unlimited
Retention	250° C / 7 days (0.28 μm <sup>2</sup> cell)	10y at 125° C extr.	10y at > 175° C
V <sub>write</sub>	4 V	1.5 V	~ 1V
Write energy	< 1fJ (per bit)	< 1fJ (per bit)	Below fJ
Mask set adder	2	NA	1
Tool capex	<b>No</b>	<b>No</b>	<b>To be discussed</b>
Solder reflow	Yes	Yes	Yes







Flash Memory Summit

# Thank you!

Contact: [stefan.mueller@ferroelectric-memory.com](mailto:stefan.mueller@ferroelectric-memory.com)