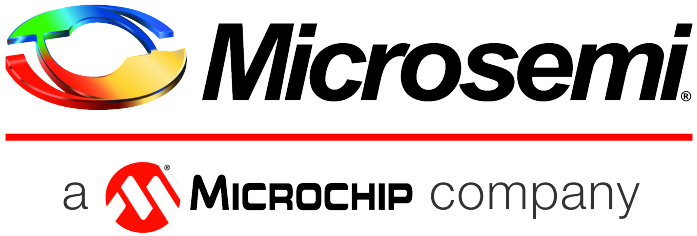


Fully Integrated LLR Calculation Flow

Lorenzo Zuolo, Alessia Marelli, and Rino Micheloni

Flash Signal Processing Lab (FSPL)

Microsemi Corporation
Via Torri Bianche, 1
20871 Vimercate (Italy)
lorenzo.zuolo@microsemi.com

New Models For Data Creation

Data creation model is evolving fast…

Users' data for users

NETFLIX

WhatsApp

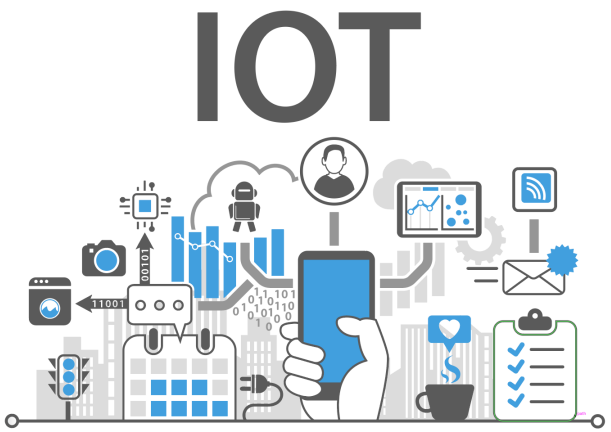
Instagram

YouTube

facebook

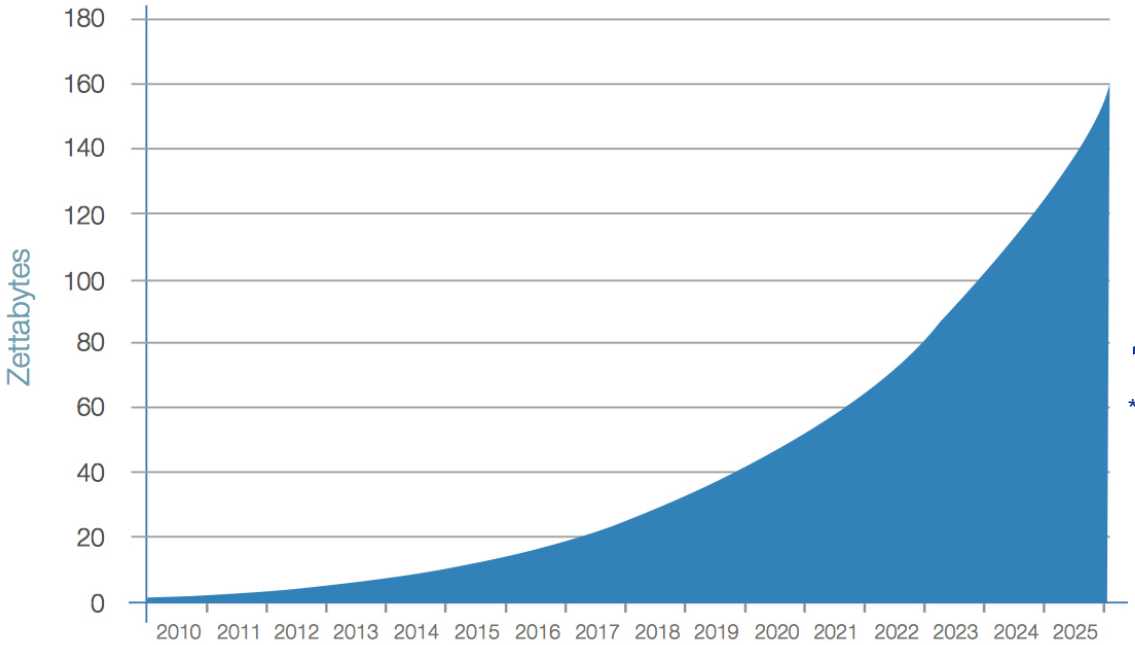
WeChat

Machines' data for machines



Flash Memory Summit

Data Growth Rate

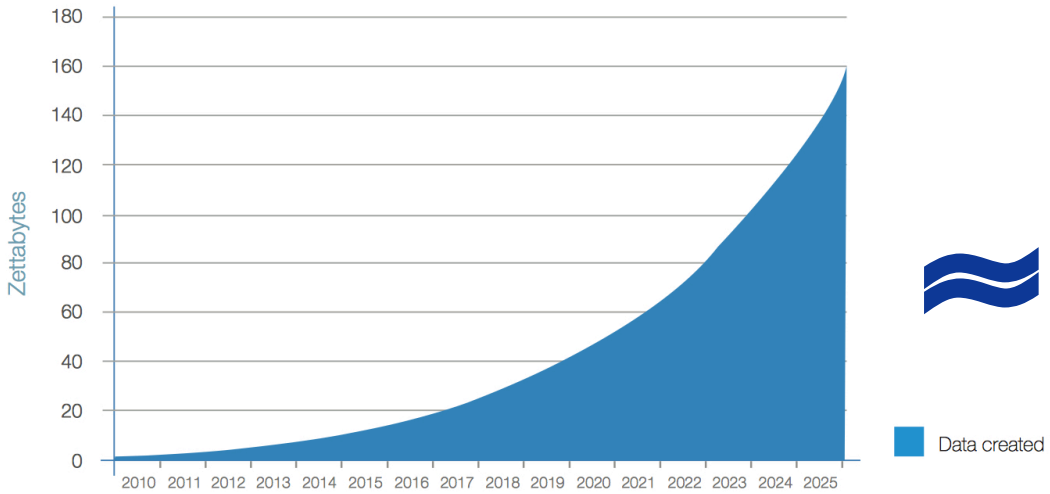


160 Zetta Bytes by 2025*

*IDC

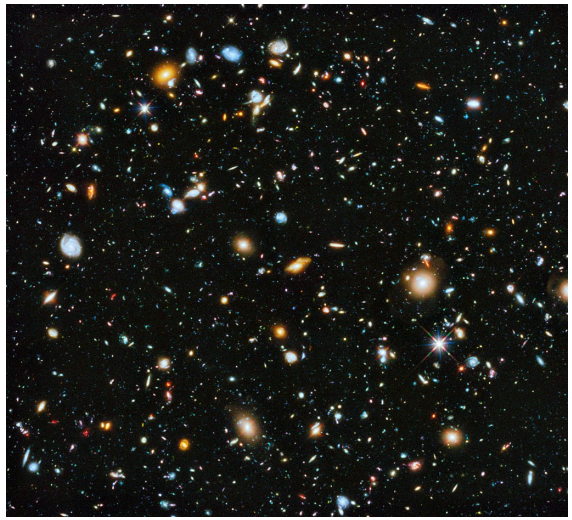
Unimaginable size… But, what if bytes were stars?

A “Universe” of Data



160 Zetta Bytes by 2025*

*IDC



300 Zetta Stars in the Universe**

**Wikipedia

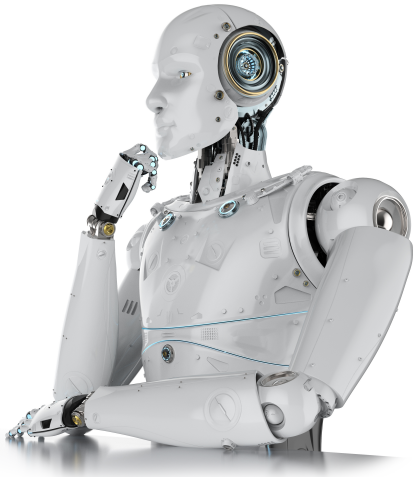
The Killer Application: "All and Now"

The usage model for stored data is also evolving quickly… We want to use ALL the collected data right NOW

Long-term archival | **Artificial Intelligence** | **Ready-to-be-processed**

SERIAL ATA

12Gb/s Serial Attached SCSI

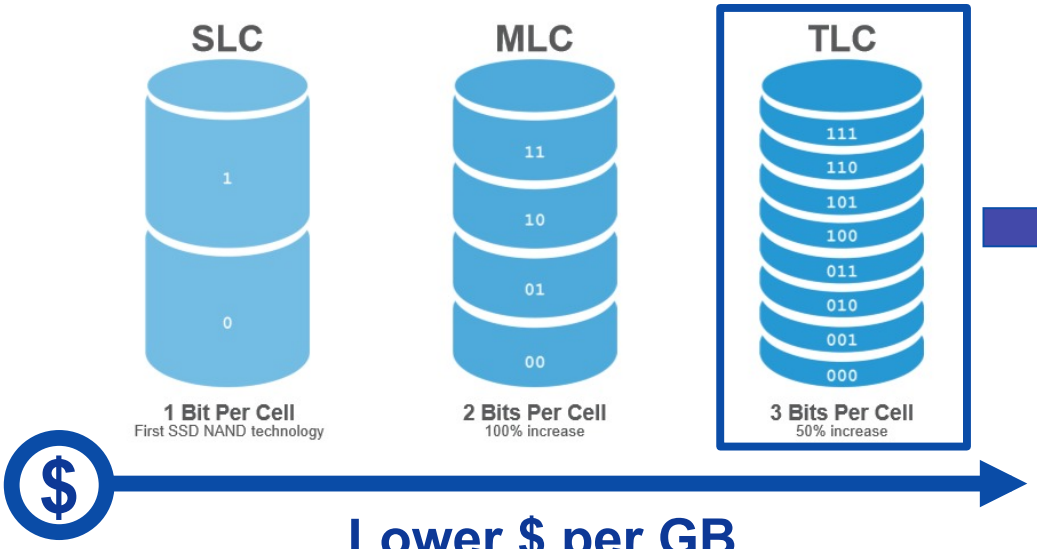


nvm EXPRESS

OpenCAPI™

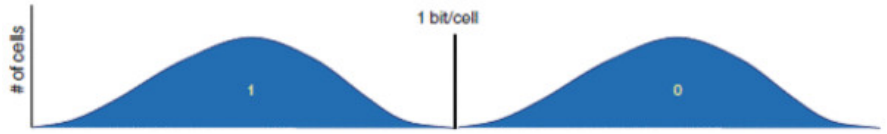
Big and Fast Data: "TLC is the new black"

Big and fast data requires dense and fast NAND flash chips



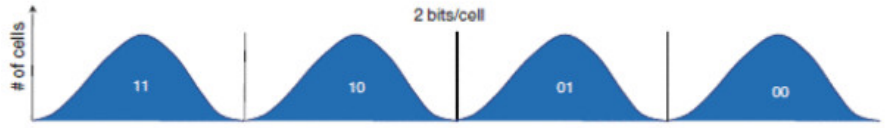
- Up to 8 Tbit per BGA package
- More than 32K blocks
- More than 2K pages per block
- Average tPROG of 3 ms
- Average tREAD of 100 µs
- Average tERASE of 10 ms

Data Reliability:
The Need for Stronger ECC



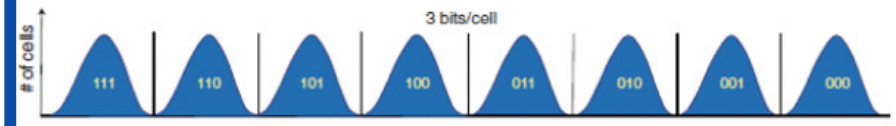
SLC → 100s of electrons per VT distribution → **BCH**

100k P/E
RBER @ EOL =1e-4



MLC → 50s of electrons per VT distribution → **BCH HARD LDPC**

20k P/E
RBER @ EOL =1e-3



TLC → 10s of electrons per VT distribution → **SOFT LDPC**

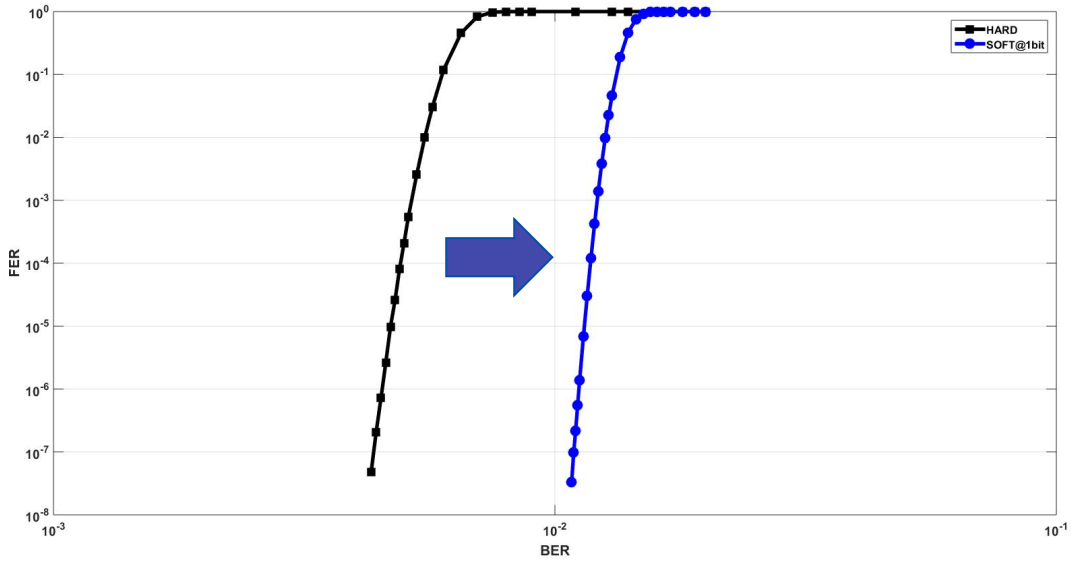
5k P/E
RBER @ EOL =1e-2

LDPC Basics

LDPCs are very good ECCs not because of the hard decoding capabilities…

- **Hard decoding is similar to BCH**
- **Soft decoding approaches the Shannon limit**

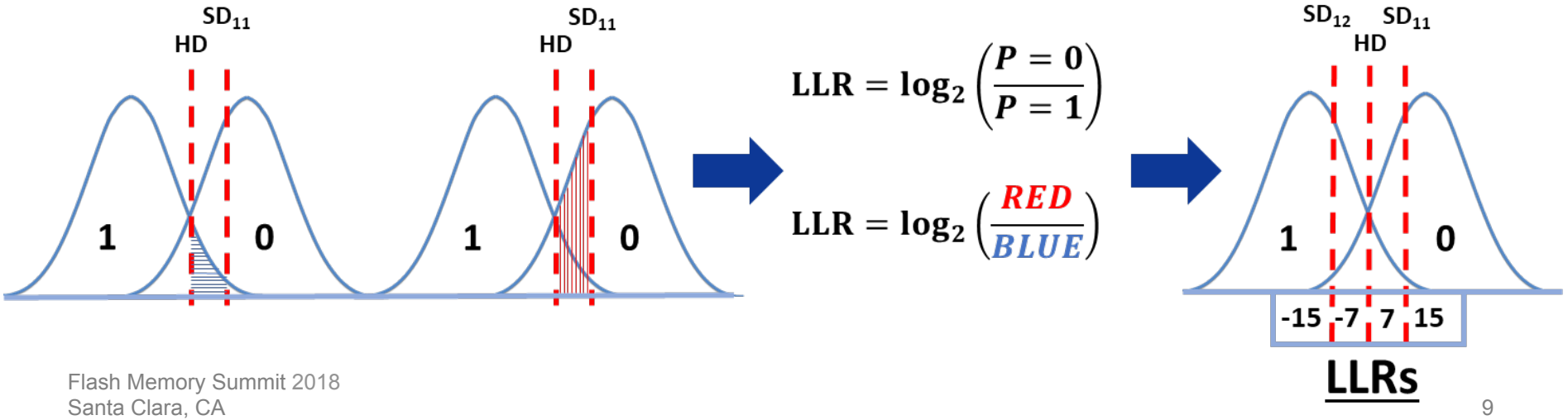
HOW?



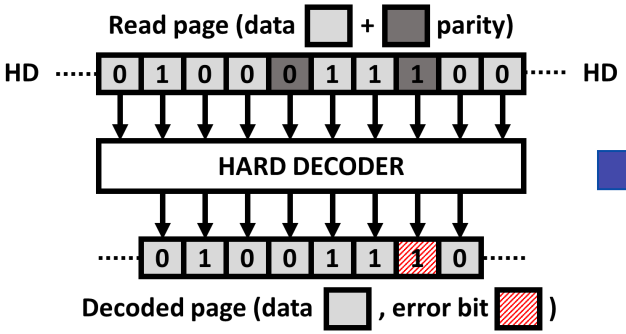
LDPC Soft Info: LLRs

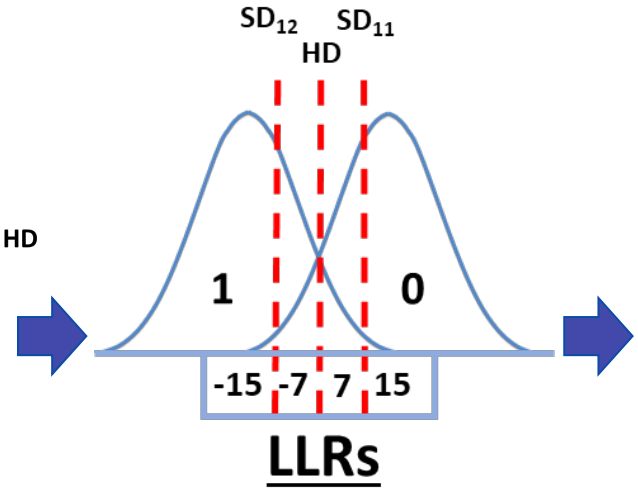
From the information theory…

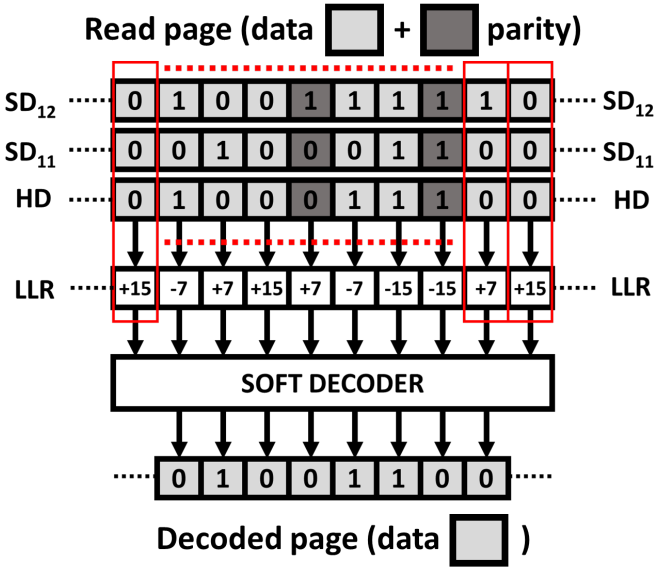
- Given a set of read references discriminating a region of the channel, the LLR is the logarithmic ratio between the probability of being a 0 and the probability of being a 1 in that specific region.



LDPC Soft Decoding







Step 1: Hard decoding failed

Bits from read codeword are used as input for the decoder

Step 2: Collect more information around the hard reference (HD) with two more reads (SD_{11} and SD_{12}) and compute LLRs

Step 3: Combine HD, SD_{11}, and SD_{12} to the corresponding LLR

LLRs are used as input for the decoder

The “devil” in LDPC soft decoding

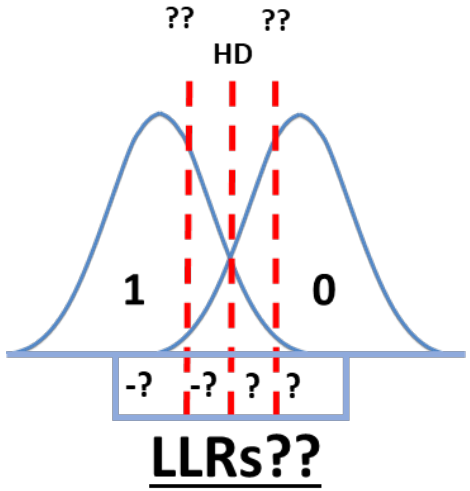
The real problem in soft decoding is neither the hardware complexity nor the decoder latency.

Calculating the right soft information is the real problem

- How many reads after the hard?
- Where should the read references be put?

Many papers solve the soft information calculation problem by:

1. Fixing an average RBER
2. Calculating the corresponding **AWGN channel**
3. Calculating the LLR values neglecting the NAND behavior



But… is it really true that AWGN channels and a NAND flash memory behave in the same way?

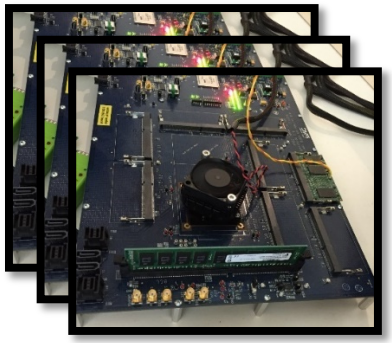
LLRs Calculation @ Microsemi FSPL: Software

- **LLR Toolbox (customer specific)**
  - Optimal read reference position calculation for best FER/power/latency
  - Raw LLR values calculation
- **LLR mapper (Microsemi Flashtec™ specific)**
  - LLR scaling for best FER/power/latency

Fully Integrated LLR Calculation Flow

Flash Memory Summit

Microsemi's char data



Char DB

100s GB per testing condition

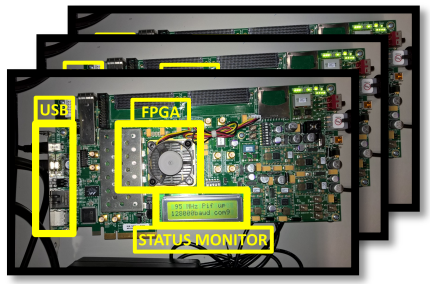
LLR Toolbox

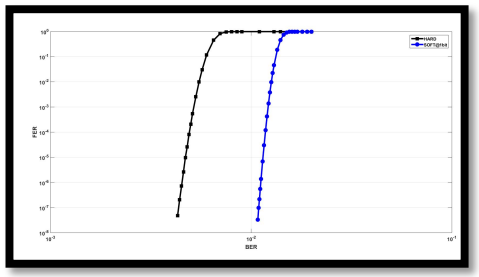
- 1 Bit Soft
- 2 Bit Soft

LLR Mapper

- Refs Position
- LLR Tables

LDPC Simulations





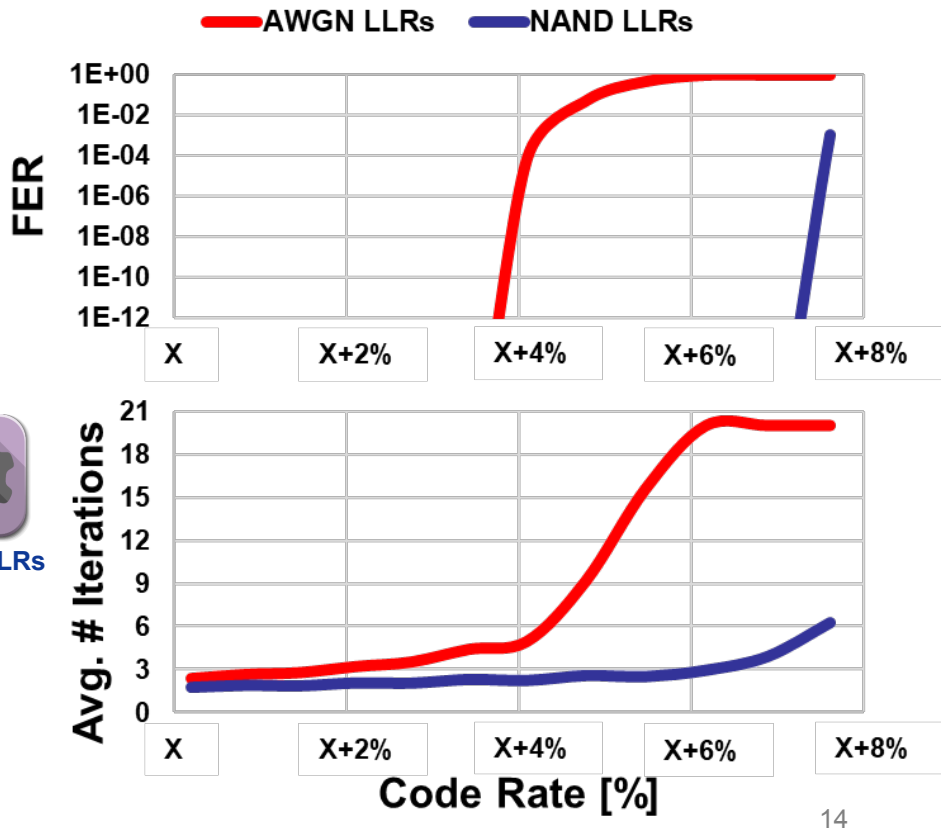
Loop until best FER/power/latency are achieved

LLRs Fab

AWGN Channel and NAND Channel

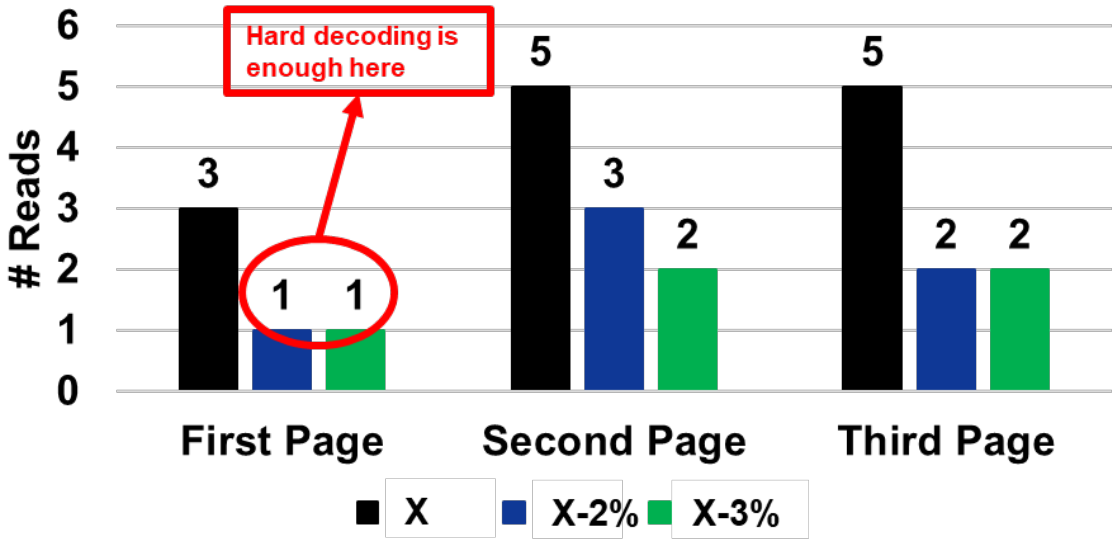
Test conditions:

- NAND stressed until EoL
- Measured RBER is 1e-2
- 100% reads are 1 bit soft



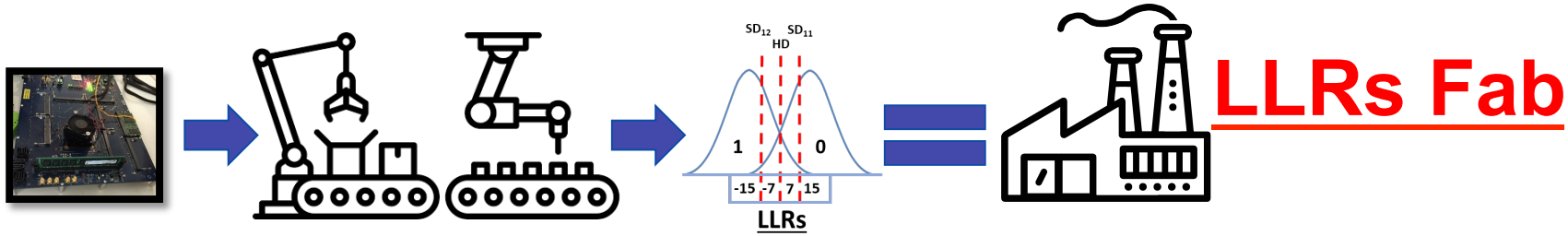
Using Optimized LLRs

Once the optimum LLRs are computed, it is possible to calculate the right amount of reads needed for a successful correction depending on the target code rate



Conclusions

- The AWGN channel and NAND channel don't match
- Being able to extract the right NAND channel is key for good LLR calculation
  → A fully integrated framework is the problem solver



- LLRs reliability depends upon the channel statistic → Huge statistic is mandatory
- With the upcoming QLC, having good LLRs will become a key point to reach the target reliability

Thank You

Q&A

Come visit us at booth #213

www.microsemi.com