The Solution to the Bit Error Non-uniformity of 3D NAND

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Manager, NAND Flash Characterization

Executive Summary

- Problem:
  - 3D NAND's bit error non-uniformity behaves much worse than 2D NAND's. This is a big challenge for error correction.
- Our Goals:
  - develop efficient techniques to reduce the bit error non-uniformity of 3D NAND to make error correction become easy.

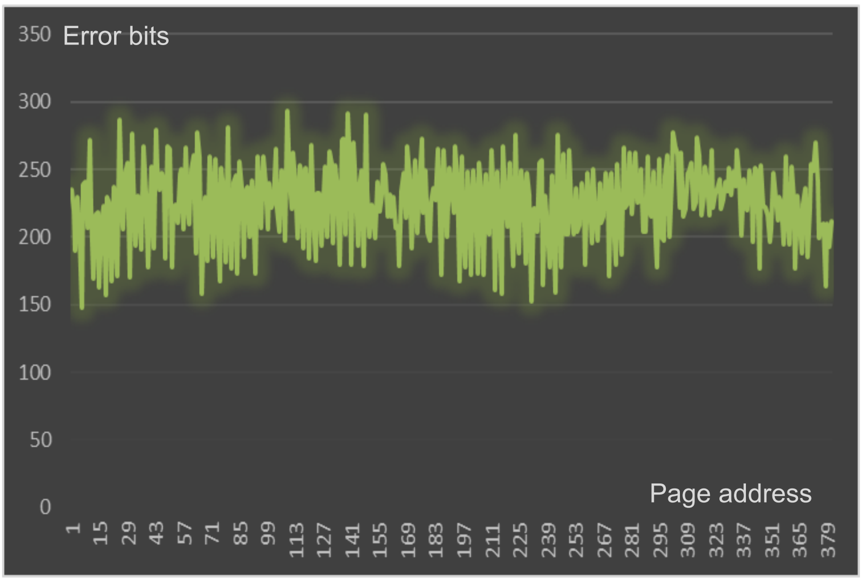
Agenda

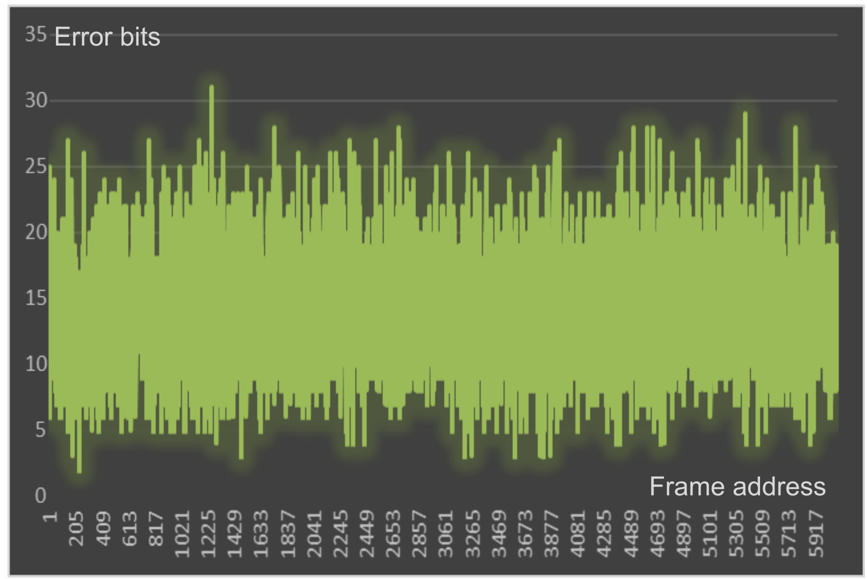
- 2D NAND bit error uniformity vs.
  3D NAND bit error non-uniformity
- The solution to the bit error non-uniformity of 3D NAND
- Summary
- About SiliconGo

Bit error distribution of 2D NAND

Read After Program	Min Bit Error	Average Bit Error	Max Bit Error
Page Bit Error	1	238	313
Frame Bit Error	0	15	32

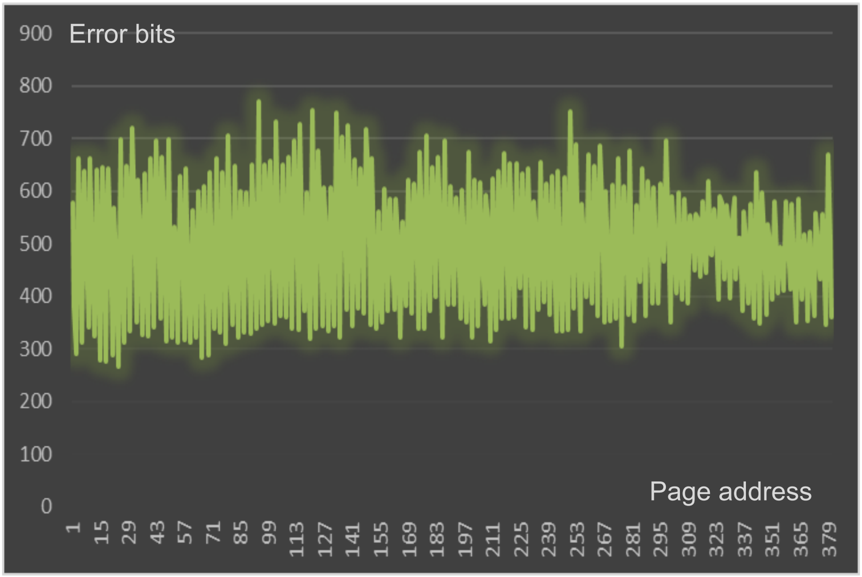
Notes:
Frame = 1024 Bytes + Parity

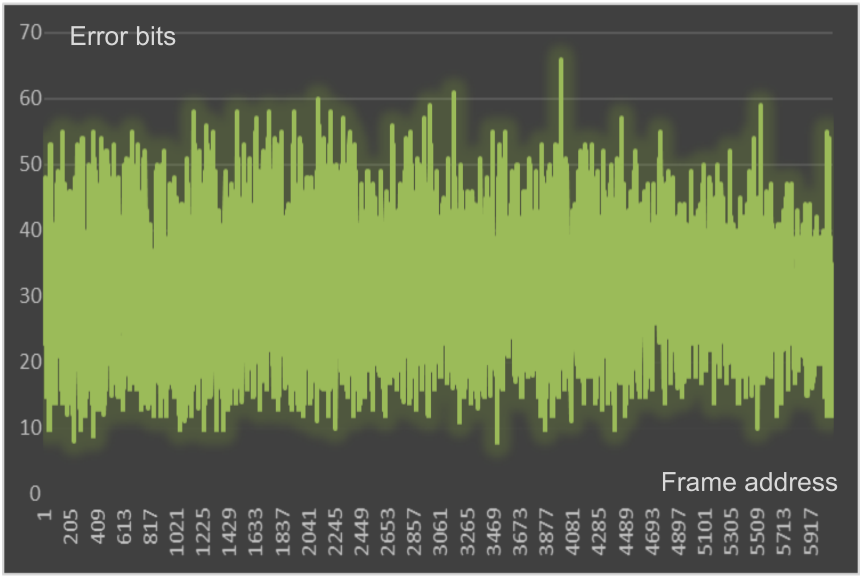




Bit error distribution of 2D NAND

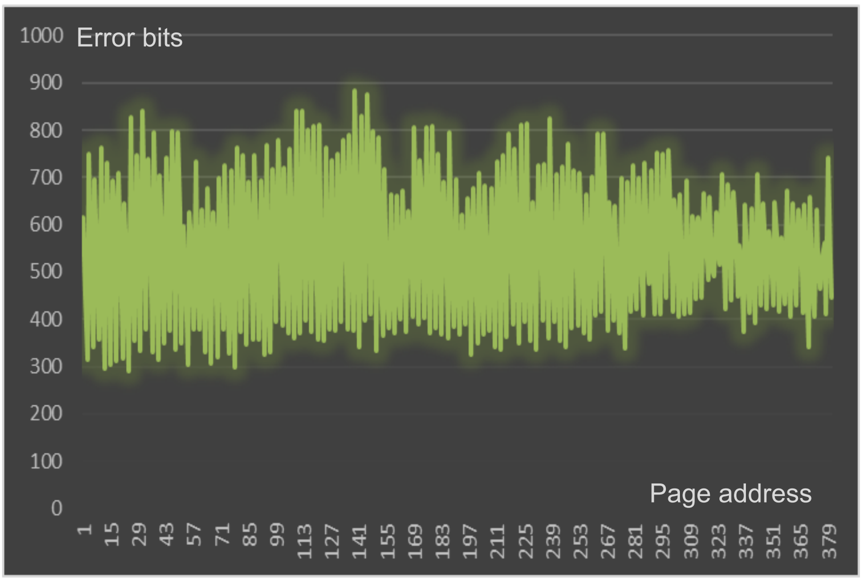
100C° 13Hours	Min Bit Error	Average Bit Error	Max Bit Error
Page Bit Error	266	498	771
Frame Bit Error	8	31	66

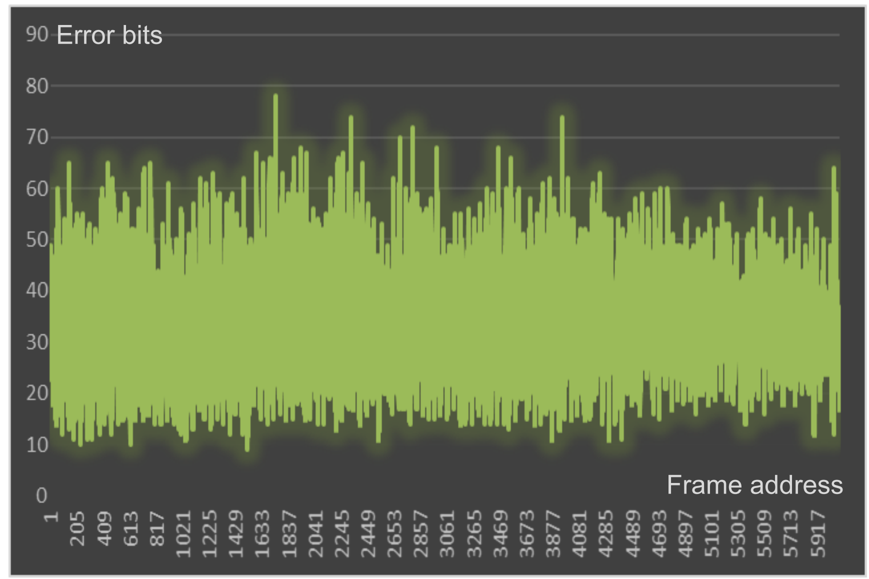




Bit error distribution of 2D NAND

100C° 26Hours	Min Bit Error	Average Bit Error	Max Bit Error
Page Bit Error	291	549	882
Frame Bit Error	9	34	78





Bit error distribution of 2D NAND

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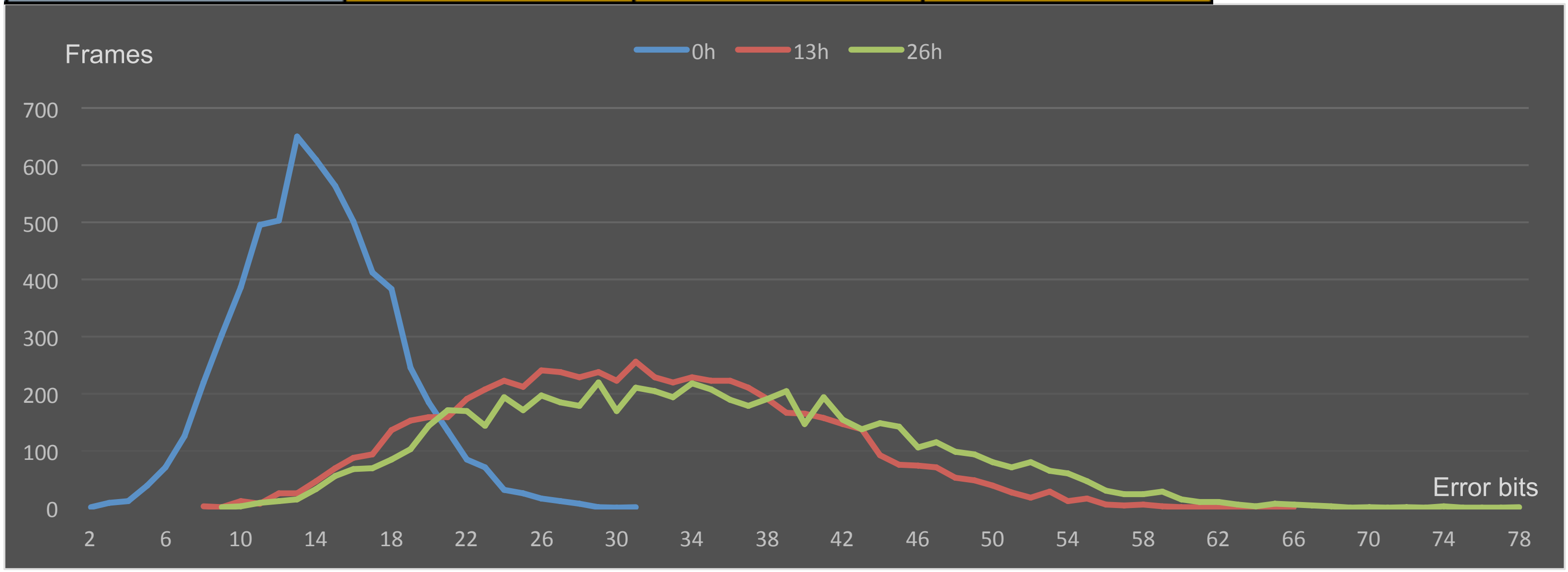
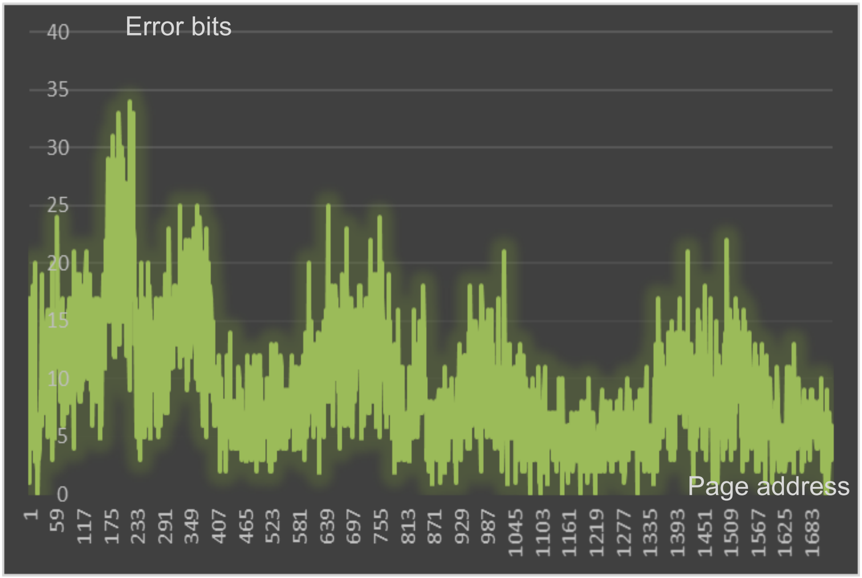
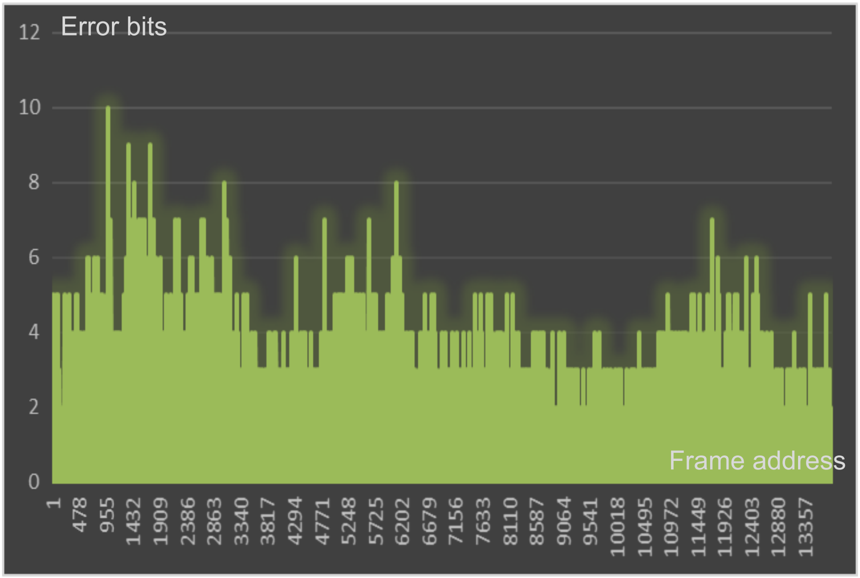


Bit error distribution of 3D NAND

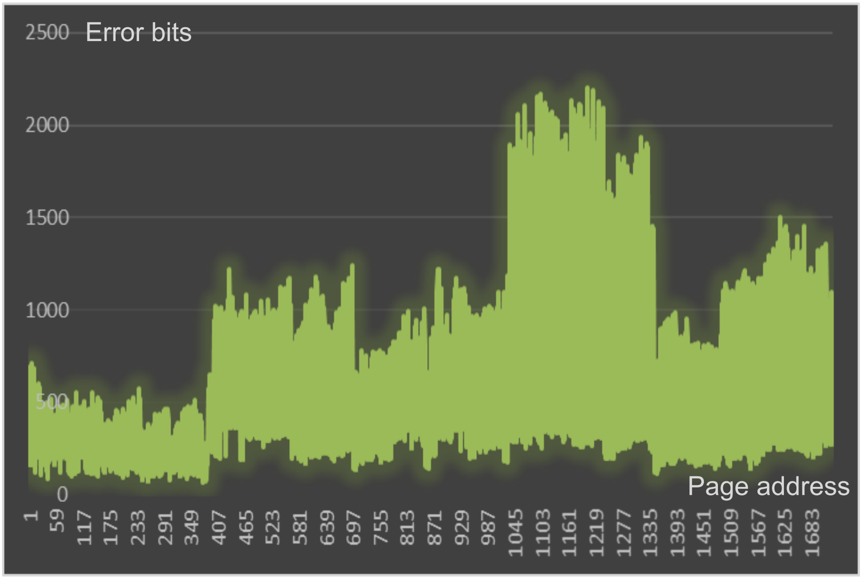
Read After Program	Min Bit Error	Average Bit Error	Max Bit Error
Page Bit Error	0	9	34
Frame Bit Error	0	1	10

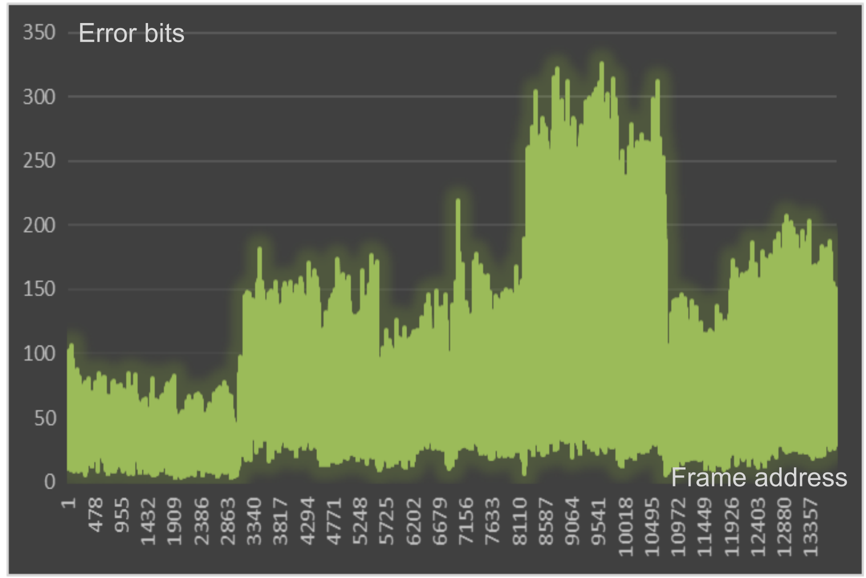




Bit error distribution of 3D NAND

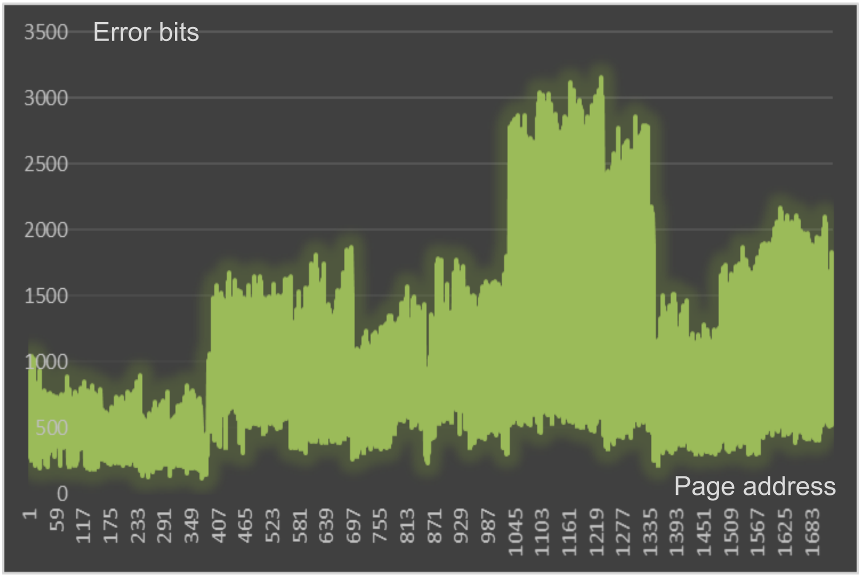
100C° 13Hours	Min Bit Error	Average Bit Error	Max Bit Error
Page Bit Error	64	699	2200
Frame Bit Error	4	87	326

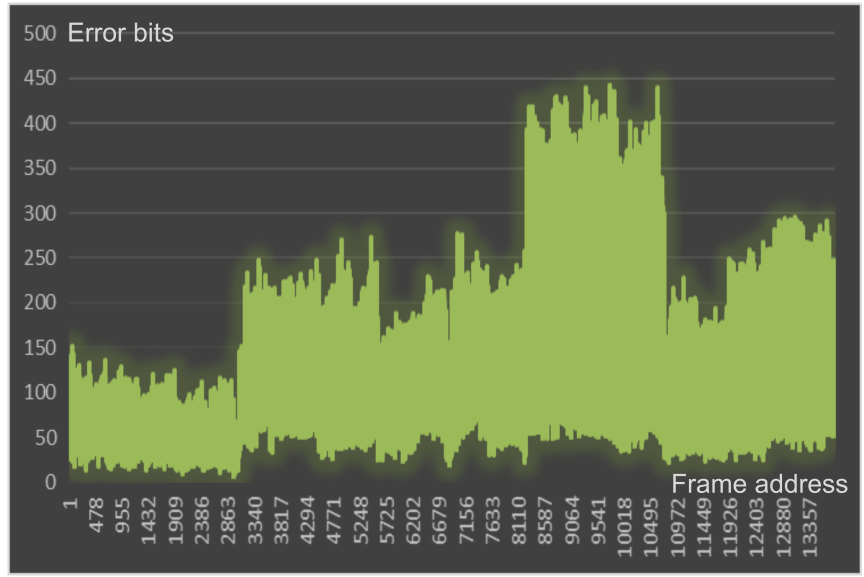




Bit error distribution of 3D NAND

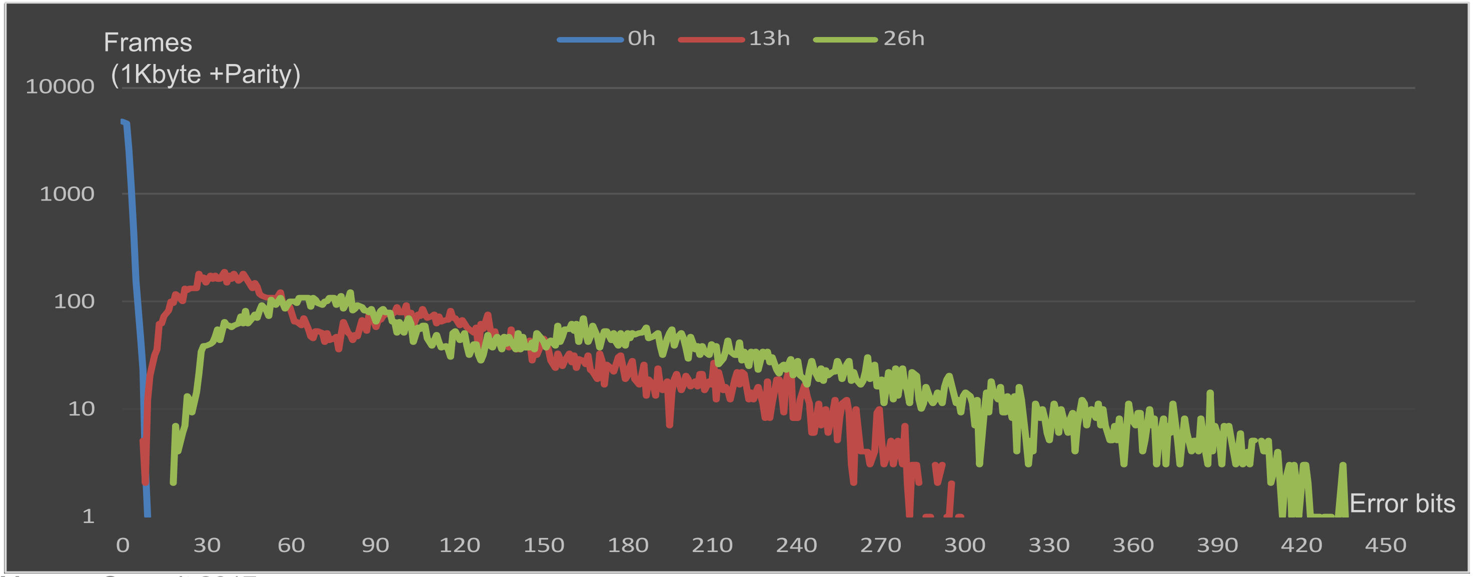
100C° 26Hours	Min Bit Error	Average Bit Error	Max Bit Error
Page Bit Error	114	1051	3153
Frame Bit Error	8	131	433





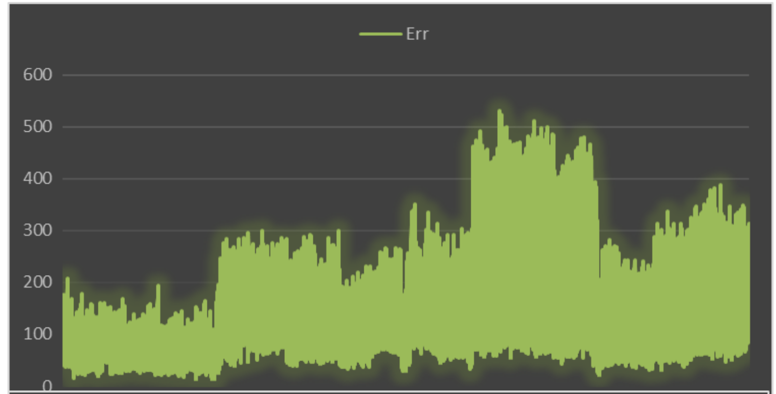
Bit error distribution of 3D NAND

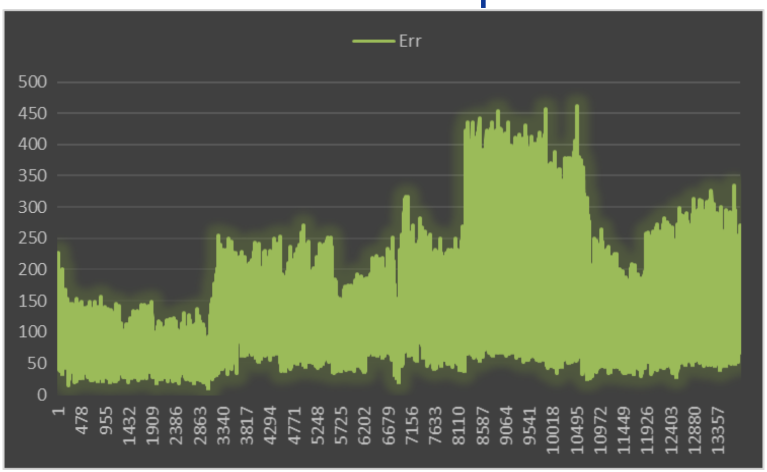
Frame Bit Error	Min Bit Error	Average Bit Error	Max Bit Error
Read after Program	0	1	10
100C° 13Hours	4	87	326
100C° 26Hours	8	131	433

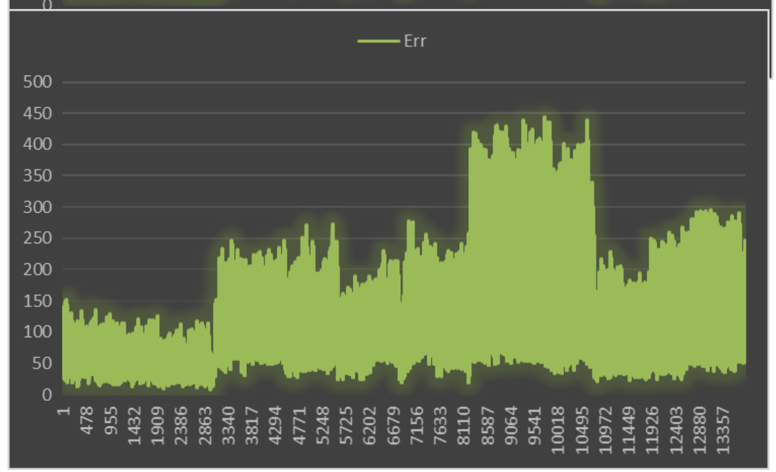


Error distribution of the same 3D NAND

Different blocks of the same 3D NAND have very similar error distributions if P/E cycles and retention are equivalent.

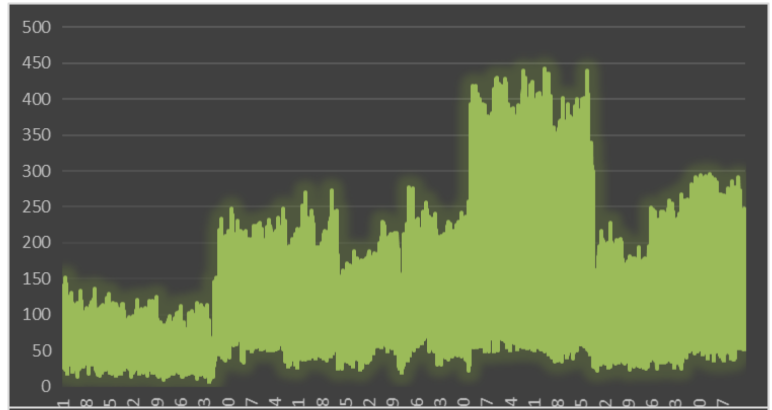


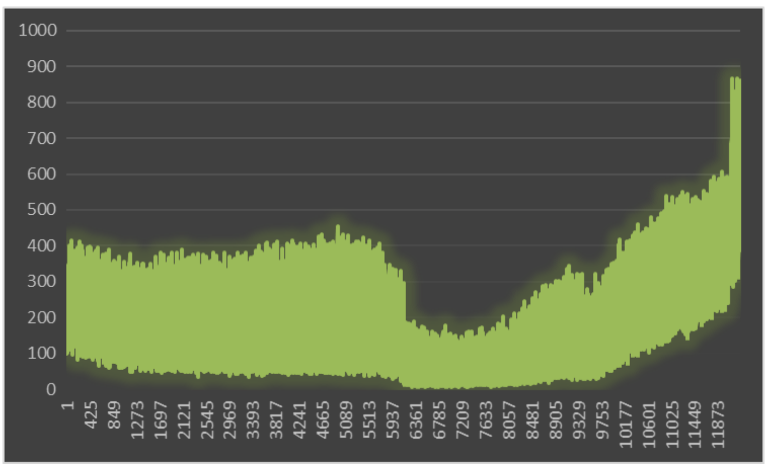


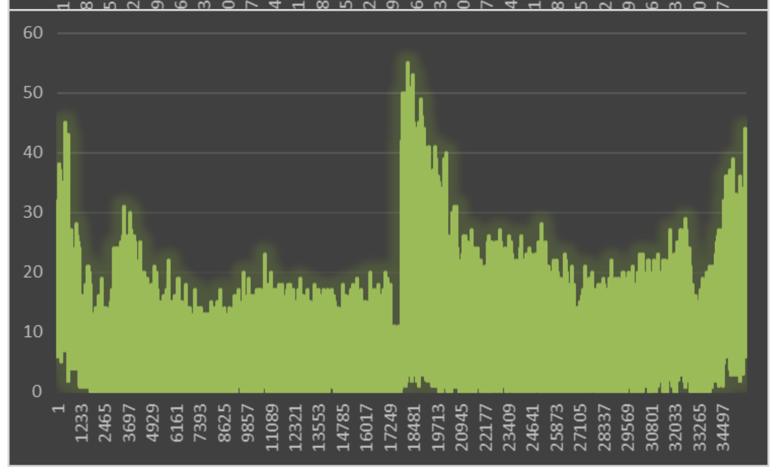


Error distribution of different type of 3D NAND

Different types of 3D NAND have different error distributions.

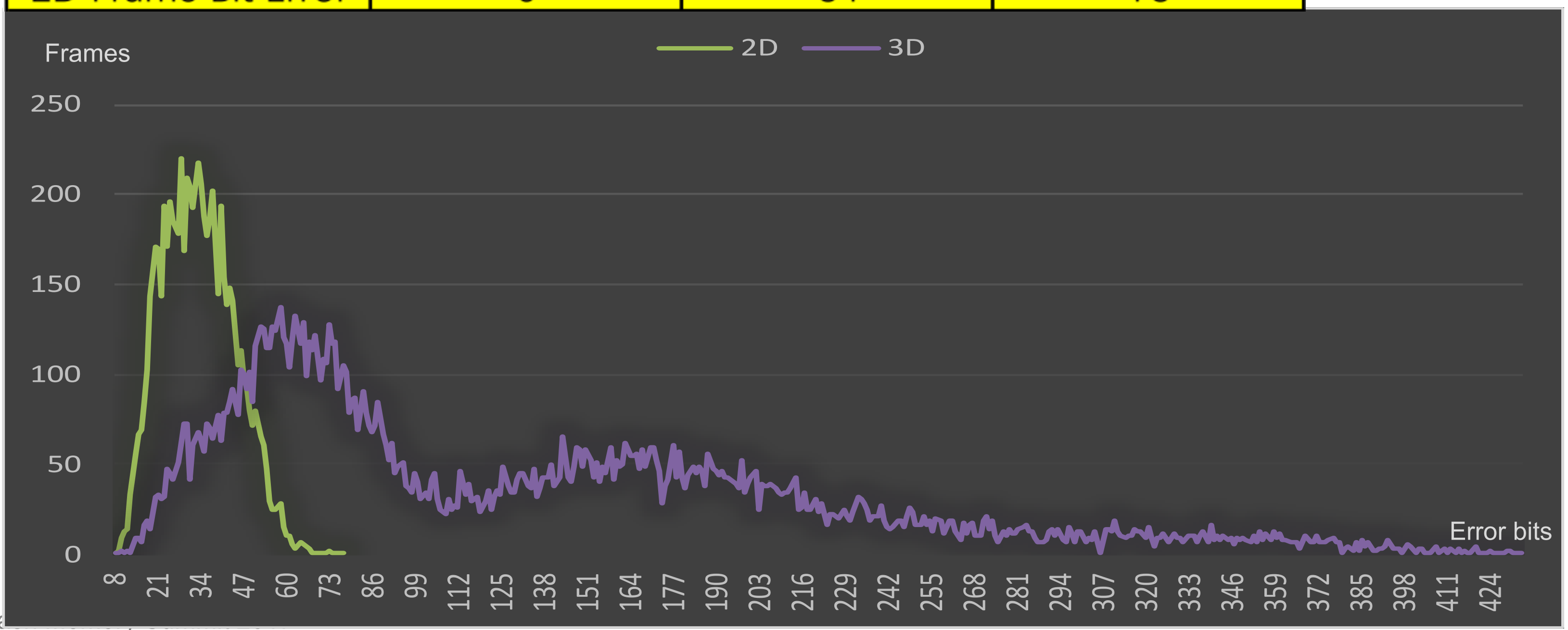






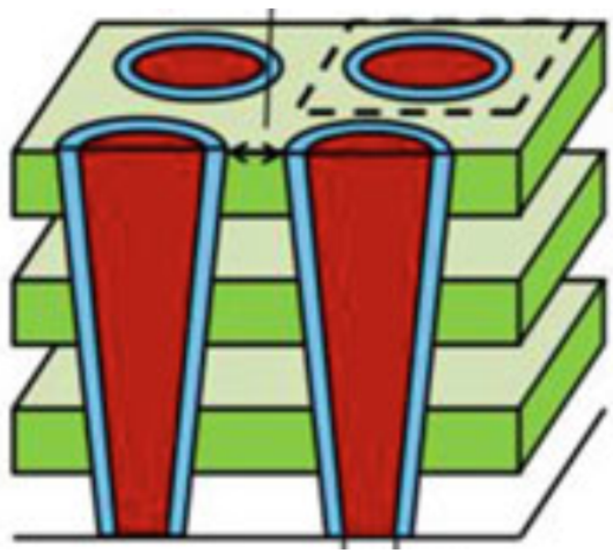
Comparison between 2D and 3D

100C° 26Hours	Min Bit Error	Average Bit Error	Max Bit Error
3D Frame Bit Error	8	131	433
2D Frame Bit Error	9	34	78



Why the error distribution of 2D and 3D are different?

- The size of 3D NAND cells are not equivalent in different layers.
- Whereas the 2D NAND cells have the same size.

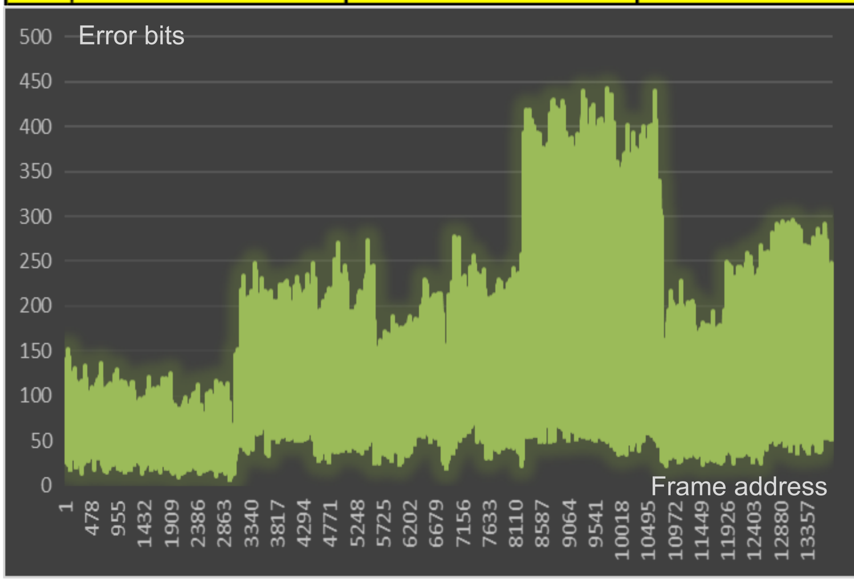


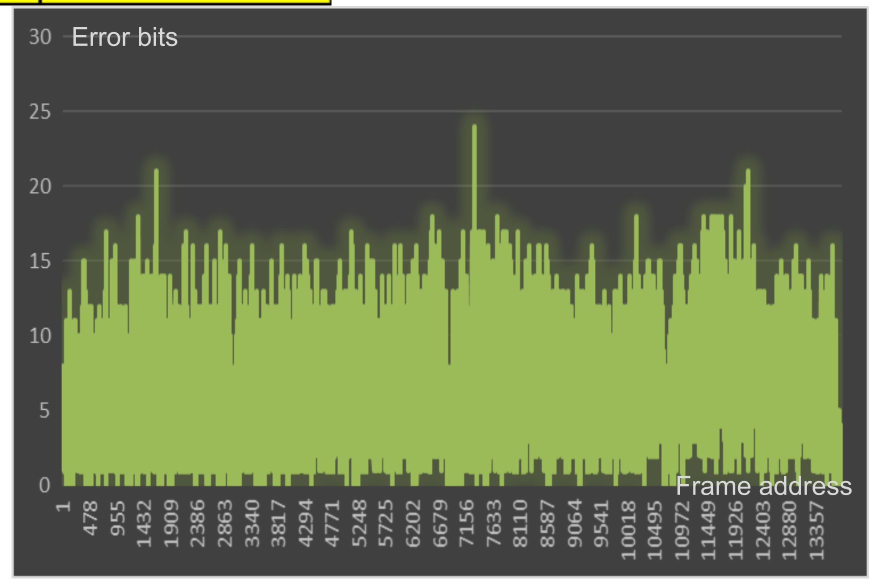
The solution to the non-uniformity of 3D NAND

- Identify the optimized read level of every WL.
- When applying the optimized read level to every WL, the non-uniformity in the 3D NAND can not be observed!

Read level: default vs. optimized

Frame Bit Error 100C° 26Hours	Min Bit Error	Average Bit Error	Max Bit Error
Default Vread	8	131	433
Optimized Vread	0	6	24





Read level: default vs. optimized

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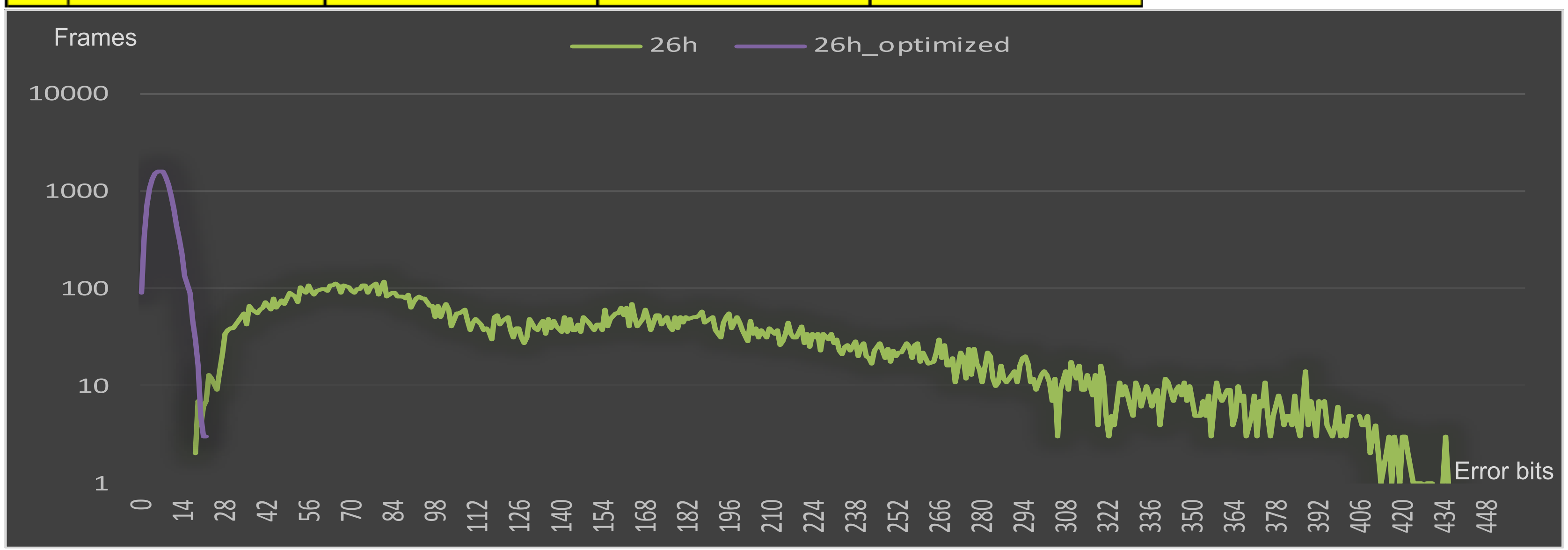
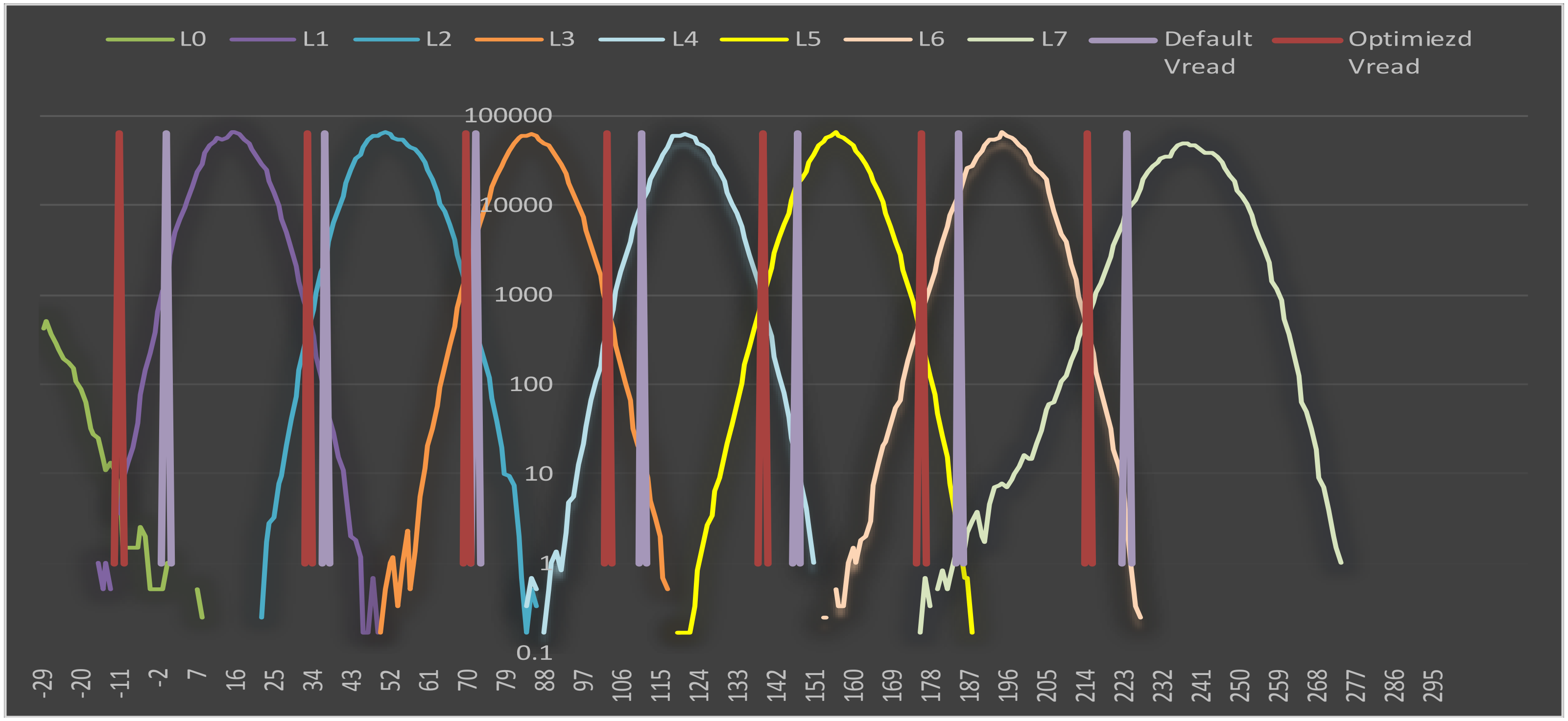


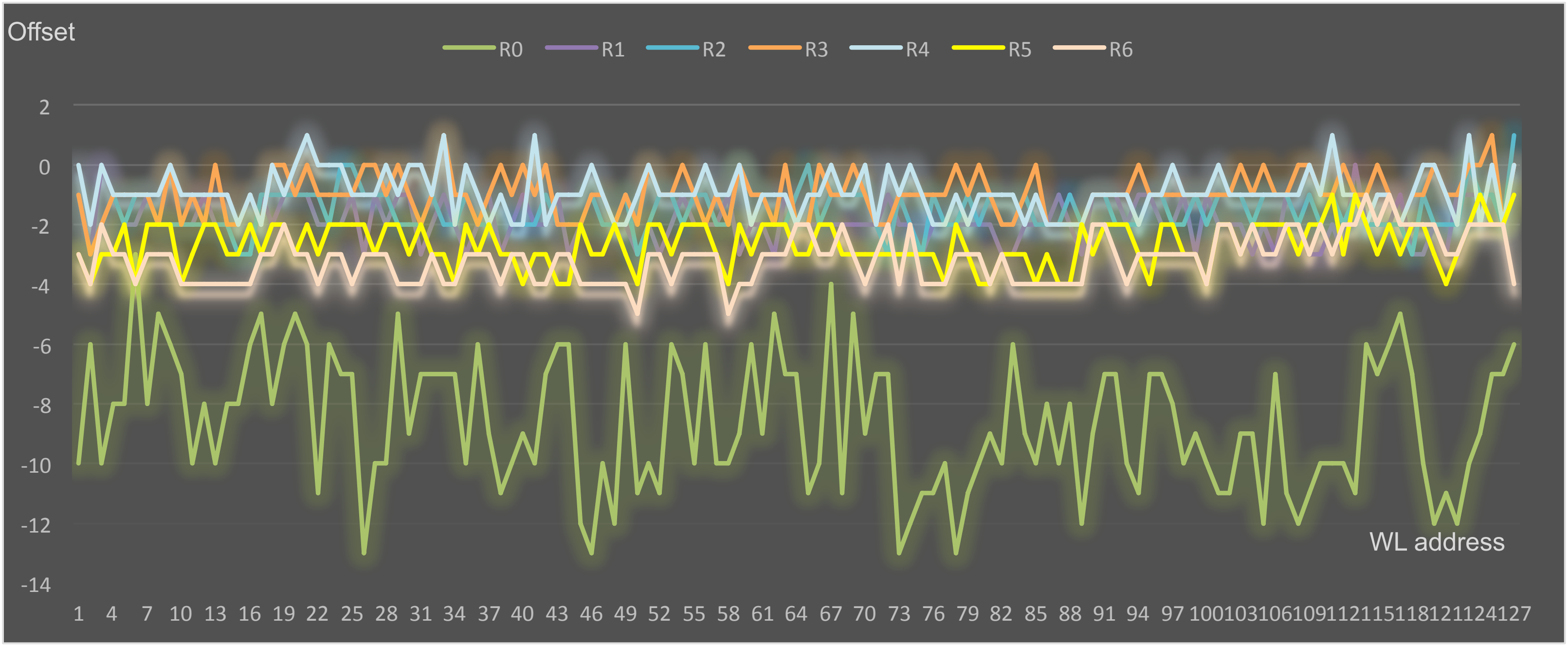
Default read level vs. optimized read level



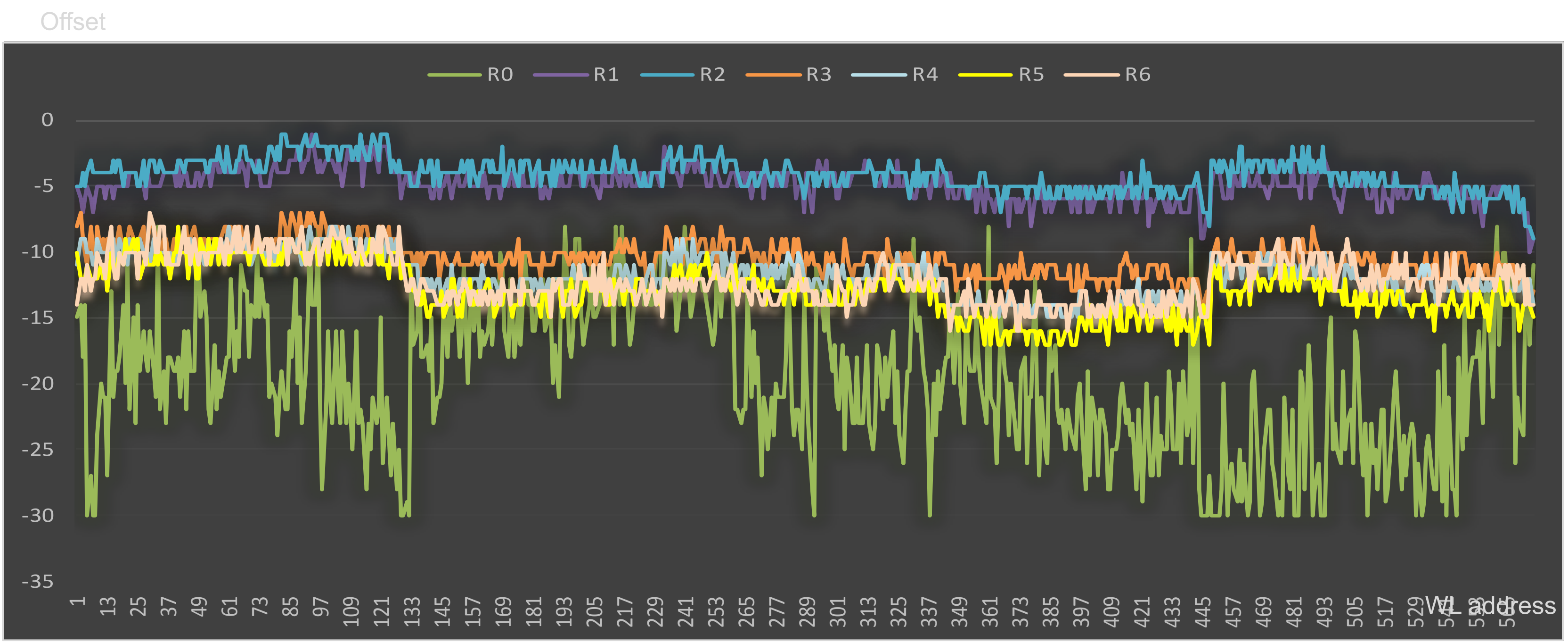
How to get the optimized read level?

- Run read retry flow for every WL
  - Slow and may not get the right read level.
- Run read calibration flow for every WL
  - Slow, but usually can get the right read level.
- Significantly reduce read speed if apply the same flow to every page read.
- Is there any fast method to get optimized read level?

Optimized read level distribution: 2D NAND



Optimized read level distribution: 3D NAND



Fast prediction method

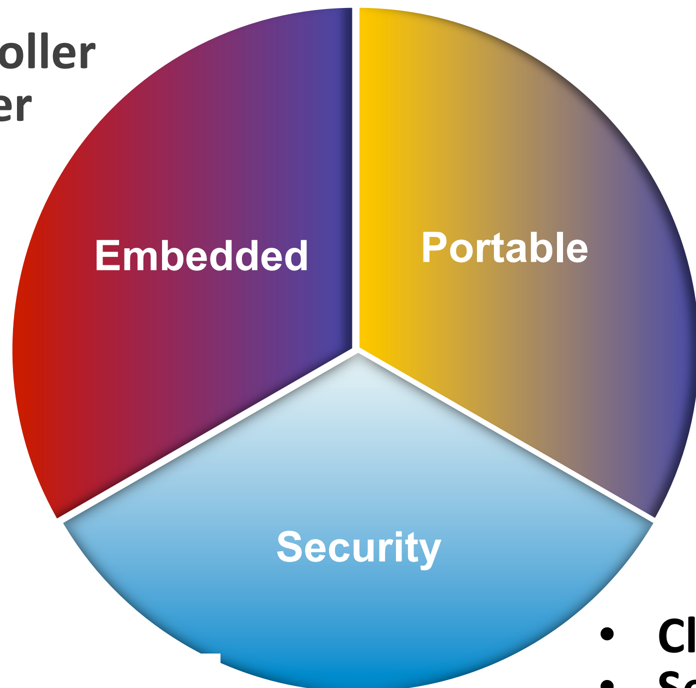
- Different blocks of the same NAND have similar optimized read level distributions, if P/E cycles and retention are same.
- 3D NAND's read level distribution is not as flat as 2D NAND's, but it has regular pattern for every block.
- In the same block, any WL's optimized read level can be predicted from other WL's read level.
- If the current page read and the last page read are not in the same block, the current read level can still be predicted from the last read level, as the two blocks of the two consecutive read operations usually have the same P/E cycles and retention.

Summary

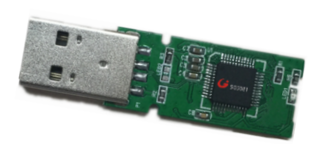
- Problem:
  - 3D NAND's bit error non-uniformity behaves much worse than 2D NAND's. This is a big challenge for error correction.
- We are:
  - developing efficient techniques to reduce the bit error non-uniformity of 3D NAND (get the optimized read level for every WL).
  - developing fast method to get the optimized read level for the current page read (predict the optimized read level based on the last page read).

About SiliconGo

- UniNAND controller
- eMMC controller
- SSD controller
- UFS controller



- USB3.1 controller
- USB2.0 controller
- SD 3.0controller
- SD 2.0controller



- Cloud bridge controller
- Security SD card controller
- Mobile payment card controller
- Security Flash disk controller

Thank you.

Feel free to email me with any questions & feedback

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