Challenges in Vertically Stackable Selectors for 3D Cross-Point Non Volatile Memories

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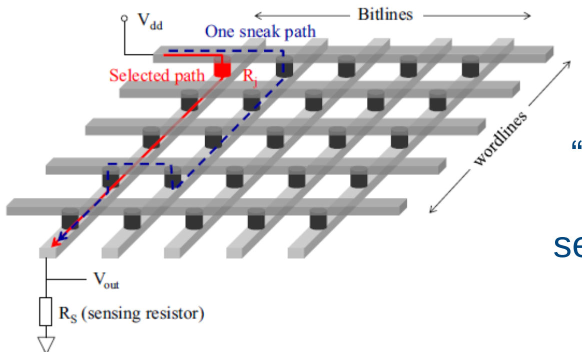
Outline

- Introduction and Background
  - 3D Cross Point Architecture – memory and selector
  - Selector Types
- NVM Device Development Challenges
- High-Throughput Experimentation Methodology
  - PVD Deposition and Etest
  - Test Vehicle Considerations
- Selector Case Studies
  - Tc screening vs composition
  - Electrical screening
- Summary

3D Cross-point Memory – Selector Architecture

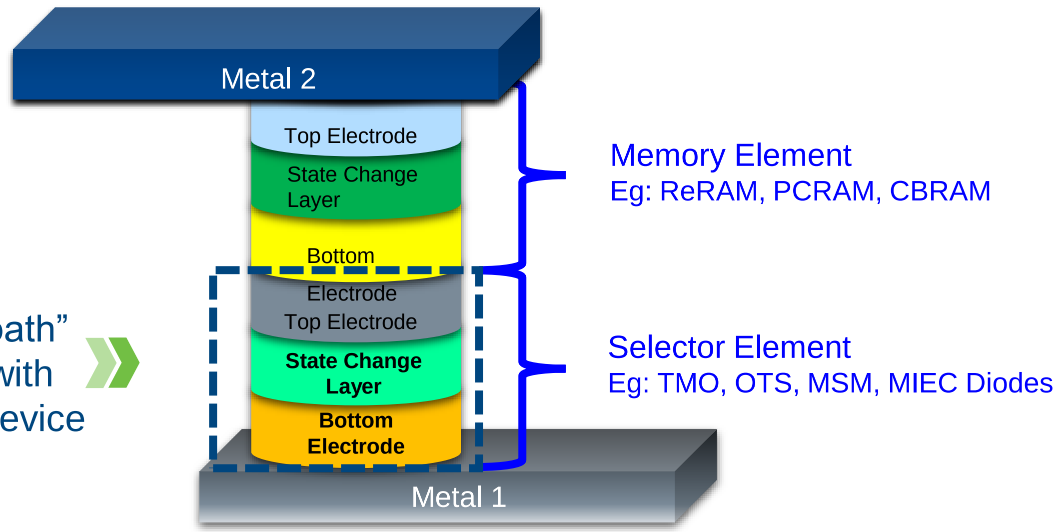
Challenges with Sneak Current Paths for 3D Cross-point Memory

Sneak current paths



* Ref: An Chen 2014 AVS TFUG Seminar

"Sneak path" solved with selector device



Generic Cross-point Memory Cell

- ❑ Selector devices are critical to eliminating sneak current paths
- ❑ Disruptive selectors needed to address performance, density and reliability requirements

Survey of NVM Selector Device Options

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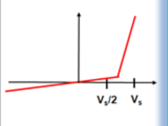
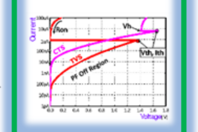
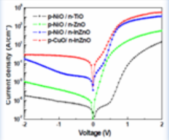
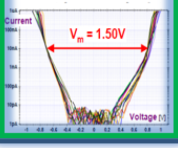
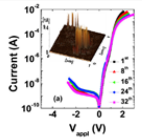
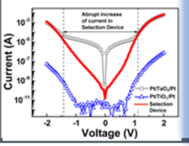
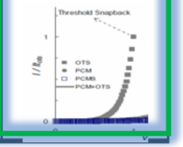
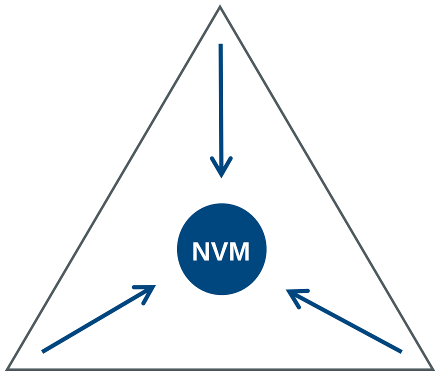
	Selector Req'ts	MSM	Oxide-PN[4]	MIEC[6]	Metal-Oxide Schottky[5]	MIIM Bi-directional Varistor[7]	Chal OTS[8]
Max Forward Current Density/ Feature Size	~$10^{6\text{-}7}$ A/cm^2	~$10^{6\text{-}7}$ A/cm^2	~5x10^4 A/cm^2@2V 0.5x 0.5um	~$10^{5\text{-}6}$ A/cm^2@1V ~80nm bot	3x10^5 A/cm^2@2V 2x2um	~3x10^7 A /cm^2 @2.5V 250nm hole	Feasibility shown for 90nm PCM
J_{FB}/J_{RB} Ratio & $J_{+Vs}/J_{+Vs/2}$ Ratio	> 10^5 > 10^3	~ 10^3	~10^4 ~100	~10^4	2.4x10^6 ~10^3	~10^4	Met PCM Req
Directionality	Uni or Bipolar	Bipolar	Unipolar	Bipolar	Unipolar	Bipolar	Bipolar
Switching Time/ Endurance	< 10ns/ > 10^8	<10ns > 10^7	10-100ns/ ?	~ 1us/ > 10^6	< 1ns ?	< 1ns/ > 10^{10}	Feasibility shown for 90nm PCM
Deposition Temp/ Thermal Stability	< 400C/ > 400C	< 400C/ > 400C	< 400C/ ?	200C/ > 400C	250C/ ?	300C/ ?	< 400C/ Issue
Typical Materials/ Stacks Used	Fab Friendly	Semiconductors	CuO/IZO NiO/IZO	Cu in Solid Electrolyte	Pt/TiO_2/ TiO_{2-x} /Pt	Pt/TaO_x/TiO_2 /TaO_x/Pt	As, Ge, Si, S, Se, Te, N
I – V Curves							

- Choice of selector devices in 3D Cross-point implementation is a trade-off between performance, reliability and ease of integration

NVM Device Development Considerations

- Filamentary based
  - O-vacancies (ReRAM)
  - Me-ions (CBRAM)
- Non-filamentary based
  - Memristor-like
  - Vacancy modulated conductive oxides
  - MIEC Selectors
- Alternative NVMs

Material/Stack



Device Structure

- Current control and selection
  - 1T1R, $1R_L1R$, 1D1R, 1R1R, 1R
- Cell design for enhanced performances

Electrical Operation

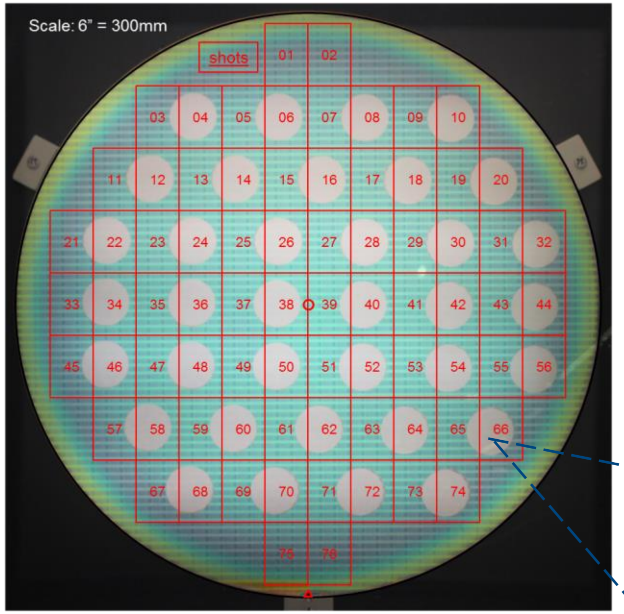
- Control of each step starting with forming
- Characterize performance vs yield vs data retention trade-offs as a function of electrical operation

❑ Disruptive NVM memories/selectors need fast and comprehensive device screening/ experimentation

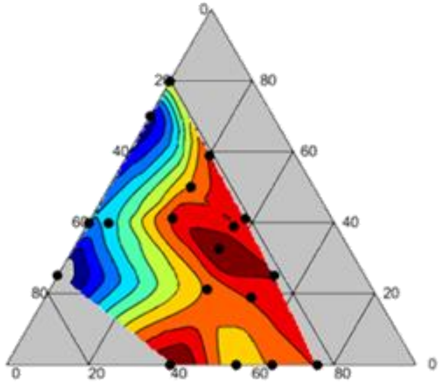
PVD Site-Isolated Deposition and Test

IMI P-30 PVD Chamber

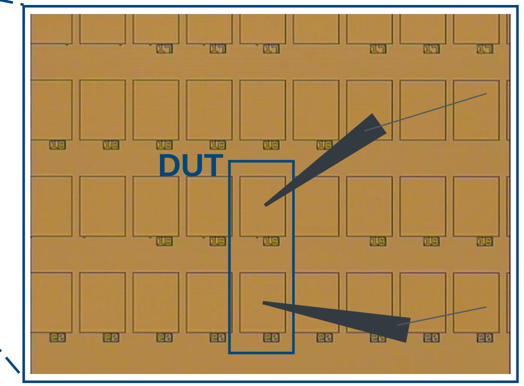
Site Deposition on 300mm wfr



Ternary Space Screen



DUT Probing



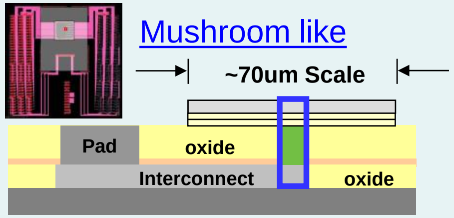
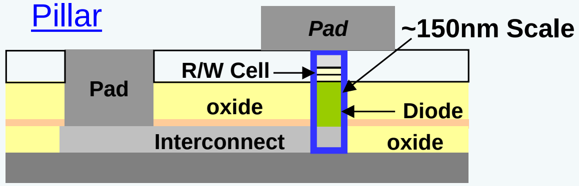
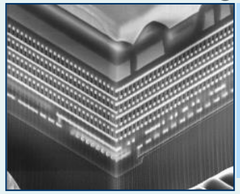
Each site is an independent experiment

- Each layer can be deposited by 1 to 5 sputter sources
- Multiple layers can be deposited at one site
- Aperture defines area where material is deposited → areas are site isolated
- Shutters for Aperture and Target prevents cross-contamination between layers & targets
- Each site composition is physically and electrically characterized

❑ Rapid deposition and screening of compositionally diverse space of interest

NVM Device Development Stages

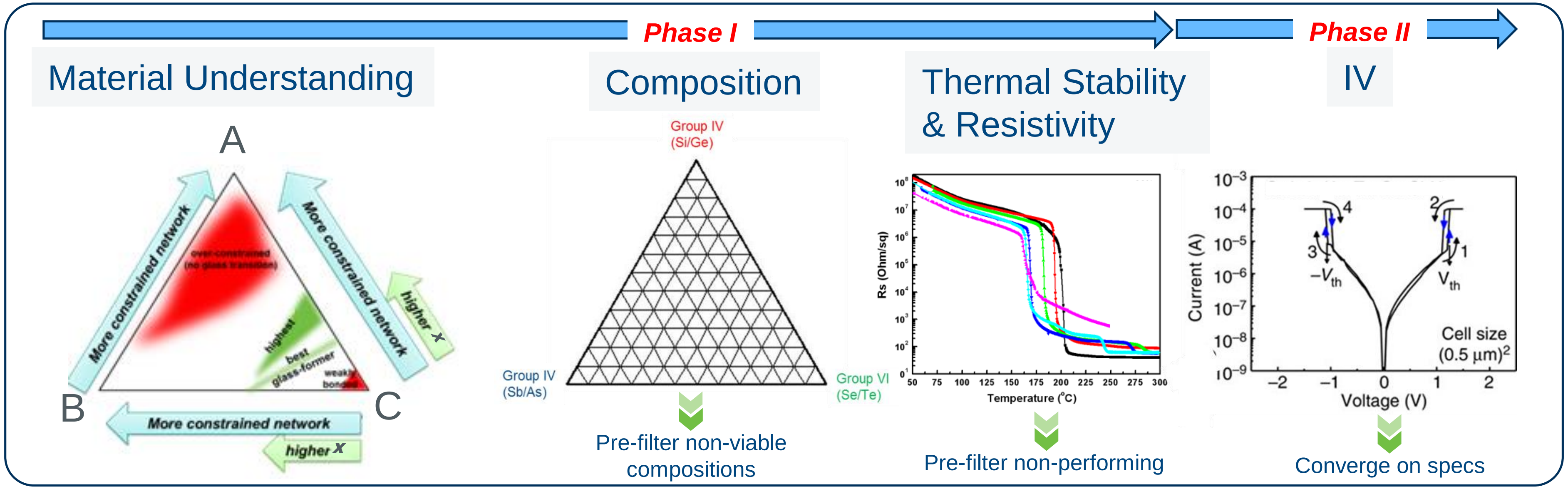
Level 1 → Level 2 → Level 3

Test Vehicle	Description	Output
Unit Films on Blanket Wafer <1 week	Materials screening, ALD and PVD unit process optimization and integration	▪ Saturation and growth curves, dep rate ▪ Physical/electrical characterization
Shadow Mask <3 days	Measure I-V at RT before/after anneal	▪ Leakage Density, Resistivity
Primary Test Vehicle 1-2 DOEs/week 16-20 COLs/DOE	Mushroom Like, BEL CD≥150nm, 1R1R, Single Bit/Mini-Array Mushroom like  	▪ Pulse P/E Power ▪ Read State Disturbance ▪ P/E Power vs Time
Secondary Test Vehicle 1 DOE/ 2-3 weeks 16-20 COLs/DOE	Column/Pillar Like, TEL= BEL CD≥150nm, 1R1R and 1T1R, Single Bit/Mini-Array Pillar  	▪ Data Retention ▪ Endurance ▪ Performance Variability
Tertiary Test Vehicle 1 DOE/ 4-5 weeks 5-10 COLs/DOE	Column/Pillar Like, TEL= BEL CD≥ Minimum 1R1R and 1T1R, Single Bit➔Large Arrays  At Dimension Memory Array	▪ Area Scaling ▪ Integration and Yield ▪ MLC and ECC

* Ref: TY Liu 2013 ISSCC

NVM Selector Screening Methodology

- Material composition space for Chalcogenide glasses exhibiting threshold vs. memory switching can be rapidly screened for physical and electrical performance.
- Explore composition space of Group IV (Si, Ge), V (As) and VI (Se, Te) compounds to develop guideline of thermal stability, resistivity, optical bandgap and I-V characteristics

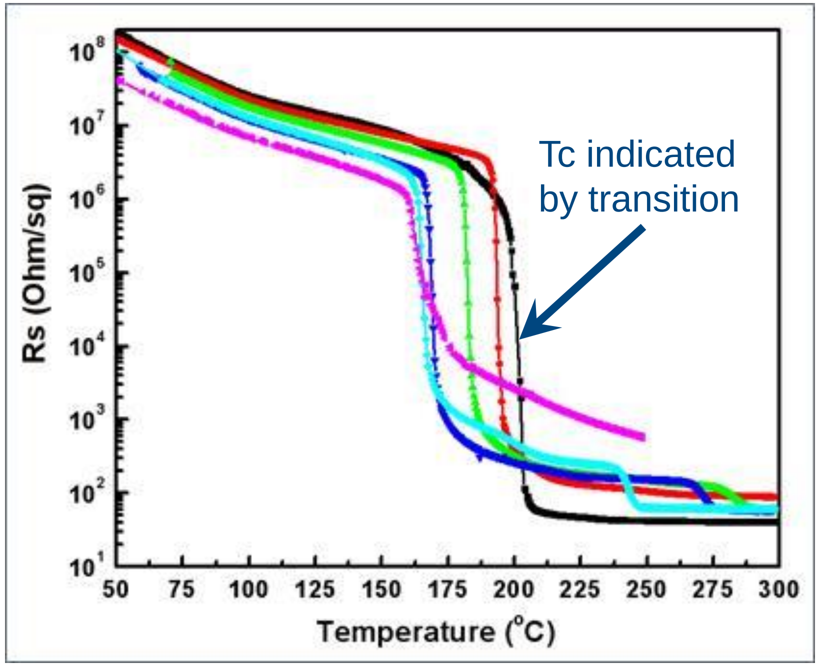


- Phase I – Composition vs. Thermal stability, crystallinity, resistivity, and optical bandgap
- Phase II – Composition vs. IV (Selected portion of Phase Diagram)

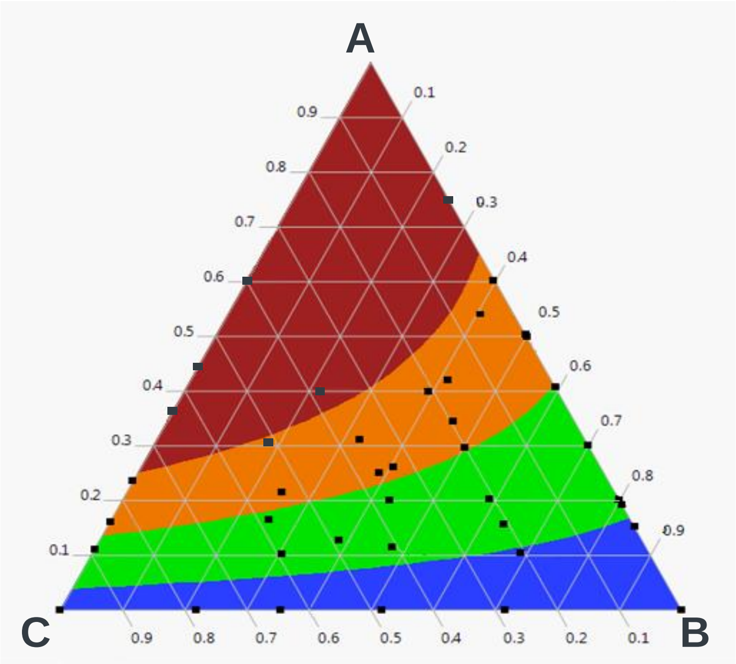
❑ Selector development is based on High-Throughput-Experimentation deposition and characterization methodology

Phase I: Rapid Screening of R_s vs Temperature

Varying composition AxByCz

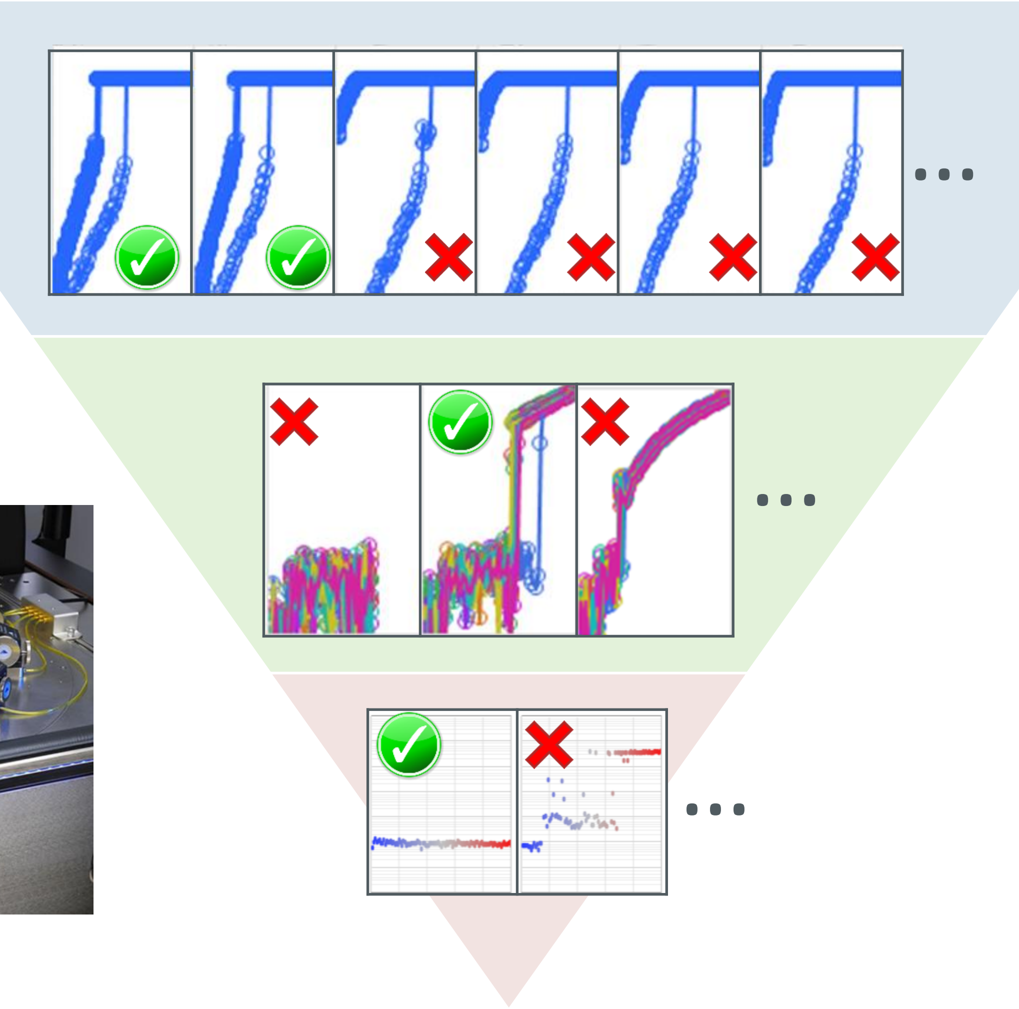


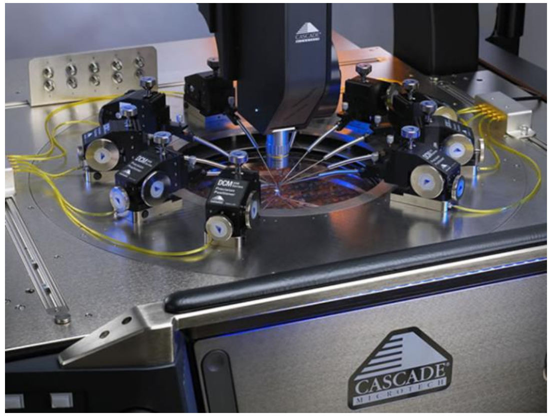
Response Surface:
Tc, Crystallization Temp



- ❑ Rapid evaluation of the composition space for Tc enables the use of Tc as a pre-filter for promising selector candidates

Phase II: Electrical Characterization





DCIV
- Level 1 screening
- All splits

Pulsed IV
- Level 2 screening
- Selected splits

Endurance
- Level 3 screening
- Champion splits

- ❑ Increasingly advanced electrical characterization used to realize screening promising selector candidates

Summary

- The move towards 3D Cross-point architecture for non-volatile memories has resulted in a need for disruptive memory and selector devices
  - Choice of selector devices is a trade-off between performance, reliability and ease of integration (fab-friendliness)
- Realization of disruptive NVM memories/selectors needs fast and comprehensive device screening/experimentation
- We propose a High-Throughput-Experimentation methodology that enables rapid new materials development and characterization for:
  - Compositionally wide material space
  - Increasingly complex electrical performance characterization
- IMI has successfully collaborated with customers to realize novel devices using this methodology

- Acknowledgments: C Chen, J Watanabe and Customer+IMI collaboration teams

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